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Design of Low Power Truncation-Error-Tolerant (TET) Adder in Digital Signal Processing

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ABSTRACT

In modern VLSI technology, the presence of all kinds of errors has become unavoidable. By adopting a rising concept in VLSI design and testing, error tolerance (ET), an error-tolerant-adder (ETA) is suggested. The ETA is able to ease the strict restriction on accuracy, and at the same time attain enormous improvements in both the power consumption and speed execution. We can compare it to its ceremonious counterparts, the suggested ETA is able to achieve more than 65% improvement in the Power-Delay-Product (PDP). There is one advantage of the proposed ETA is that it can tolerate certain amount of errors.

Key Words: ET, ETA, VLSI, Digital Signal Processing (DSP)

INTRODUCTION:

In conventional digital VLSI design, we can assume that a usable circuit or system should always provide definite and accurate results. But these perfect operations are seldom needed in our non digital worldly experiences. Now the existing world accepts "analog computation," which gives "good enough" results rather than completely accurate results. The data treated by many digital systems can already hold errors. In some applications, such as, a communication system, the signal (analog) coming from the outside world must first be sampled before being converted to digital data. Then the digital data processed and transmitted in a noisy channel before converting back to an analog Signal. While in this process, errors can occur anywhere.

Based on the characteristic of digital VLSI design, some new concepts and design techniques have been suggested. It includes the concept of error tolerance (ET) and the PCMOS technology. The definition says, a circuit is error tolerant if:

1) It comprises defects that cause internal and external errors and

2) The system that comprises this circuit produces acceptable results. Also, the "imperfect" property looks to be not appealing. The need for the error-tolerant circuit was foretold in the 2003 International Technology Roadmap for Semiconductors (ITRS). Therefore, to deal with error-tolerant problems, some of the truncated adders/multipliers have been reported, but are not able to perform well in its area, speed, power, or accuracy.

Naturally, not all digital systems can occupy the error-tolerant concept. Now a day in digital systems such as control systems, the precision of the output signal is extremely important, and this refuses the use of the error tolerant circuit. For many digital signal processing (DSP) systems that process signals relating to human senses such as sight, smell, hearing, and touch, for e.g. we can take, the image processes and speech processing systems, where the error-tolerant circuits may be applicable.

ETA – "ERROR-TOLERANT ADDER"

Before giving description about the ETA, the definitions of some normally used terminologies shown in this paper are given as follows:-

a) OE: (Overall error):- OE = $| R_c - R_e |$, Here R_e is the result obtained by the adder, and R_c denotes the correct result.

b) Accuracy (ACC): It is defined as: ACC = $(1-(OE/R_c)) \times 100\%$. Its value ranges from 0% to 100%.

c) Minimum acceptable accuracy (MAA): Minimum acceptable accuracy is just that threshold value. Hence, the result we have obtained, whose accuracy is higher than the minimum acceptable accuracy is called acceptable result.

d) Acceptance probability (AP): Acceptance probability is the probability that the accuracy of an adder is higher than the minimum acceptable accuracy. It can be

expressed as AP = P (ACC > MAA), where its value ranging from 0 to 1.

1. Arithmetic Addition

In a conventional circuit like adder, the delay is mainly assigned to the carry propagation chain along the critical path, from the least significant bit (LSB) to the most significant bit (MSB). A significant proportion of the power consumption of an adder is due to the glitches that are caused by the carry propagation. Hence, if the carry propagation can be eliminated or restricted, a great improvement in speed and power consumption can be attained. In this paper, we propose, an innovative and new addition arithmetic that can attain great saving in speed and power consumption. The new type of arithmetic addition can be illustrated in Fig. 1 via an example. First of all we split the input operands into two parts: an accurate part that includes several higher order bits and the inaccurate part that is made up of the remaining lower order bits. It is not necessary that the length of each part to be equal. The addition of each part in this process starts from the middle (joining point of the two parts) toward the two opposite directions at the same time. From the figure we can take the example, it has the two 16-bit input operands, A = "1011001110011010" (45978) and B = "0110100100010011" (26899), are bifurcated or split up equally into 8 bits each for the accurate and inaccurate parts.

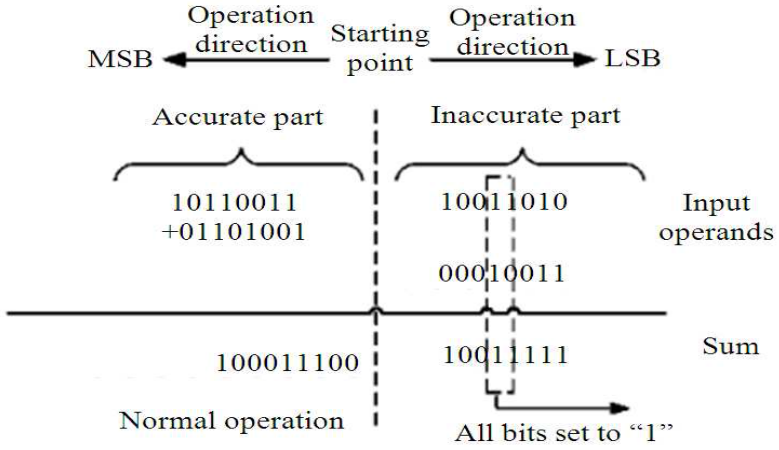

Figure 1: Arithmetic addition

2. Requirement for Error-Tolerant-Adder (ETA)

Increasingly huge data sets and the need for instant response need the adder to be large and fast. The traditional adder like ripple-carry adder (RCA) is thus no longer suitable for large adders because of its low-speed execution. There are different types of adders, like CSK (carry-skip adder), CSL (carry-select adder), and CLA (carry-look-ahead adder), are developed. Likewise, there are so many low-power adder design techniques that have been proposed. Even so, there are always trade-offs between speed and power. For this problem the error-tolerant design can be a possible solution. By sacrificing some accuracy, the error tolerance adder can achieve great improvement in both the power consumption and speed performance.

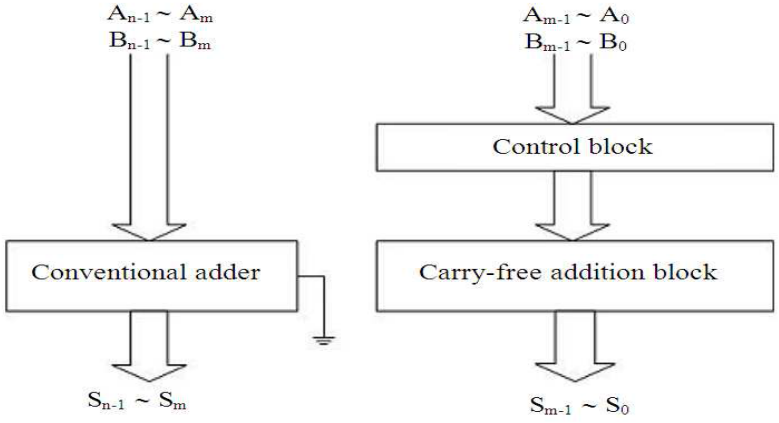

Figure 2: Hardware implementation of the ETA

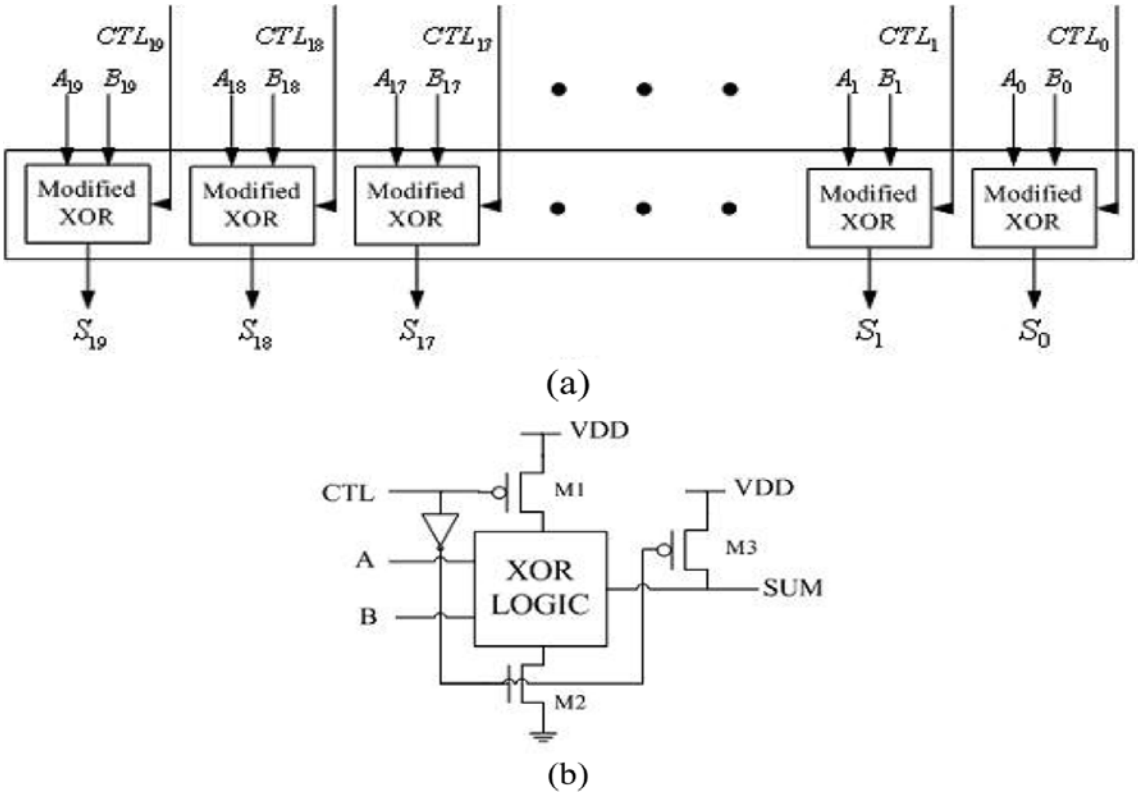

Figure 3: Carry-free addition block. (a)Overall architecture and (b) schematic diagram of a modified XOR gate.

3. CONCLUSION:

In this paper, error tolerance is introduced in VLSI design. A new type of adder, the error-tolerant adder, which have certain amount of accuracy for significant power saving and performance improvement, is proposed. The possible applications of the ETA fall mainly in areas where there is no strict requirement on accuracy or where super low power consumption and high-speed performance are more important than accuracy. We can take an example, in the DSP application for portable devices such as cell phones and laptops.

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