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A 16bit 31µw Resetting 2nd Order ∑∆ Modulator in 130 nm Technology

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ABSTRACT
High-resolution, moderate-speed, calibration-free analog-to-digital converters (ADCs) are becoming increasinglydifficult to design in low-voltage nanometer-scale CMOS processes.We proposedADC architecture based on a resettingmodulator that achieves high resolution, despite poor componentmatching. The design utilized one pipelines a second-order resetting modulator and a10b cyclic ADC. The device achieves 16b resolution. It consumes 31µW from a 1.8 V supply.The whole analysis done in 130nm technology.

***Key words*:** ADC, high-resolution, Resetting ∑∆ modulator, Quantizer, Comparator,D flip- flop, FIR filter.

1. INTRODUCTION

In recent years, high-resolution analog-to-digital conversion based on sigma-delta (Σ-∆) modulation has become common in many measurement applications including seismic, biomedical and harsh environment sensing. Oversampled sigma-delta modulation has gained much popularity in analog to digital conversion application for their good performance in high frequency, low consumption, low supply voltage and low silicon area occupation. Device scaling in modern CMOS technology enables high-speed conversion, but high-resolution is hard to achieve[1].Continuous-time (CT) ∑∆ADCs suffer from the requirement of RC time-constant calibration andare sensitive to clock jitter [6]. Switched-capacitor (SC)∑∆ ADCs employ a low over-sampling ratio (OSR) and multi-bitfeedback DACs to achieve high-bandwidth, but calibrationand/or dynamic element matching of the feedback DACs isrequired to maximize performance [2].∑∆ ADCs also required digital decimation filter of considerable speed [6].

A resetting converter, also known as single-shot or incremental [8] converter, is essentially a ∑∆ADC in which the modulator is reset after a pre-determined number of clock cycles. Another type of resetting ADC, known as an extended counting converter uses reuse able hardware and uses high-resolution, compact, and low-power ADC both employs a first order resetting modulator.

ADC architecture based on a resetting modulator achieves high resolution, despite poor component matching .A resetting is the modulator reset after a predetermined number of clock cycles.Resetting removes the memory of the modulator and enables the converter to function as a Nyquist converter. In this way resetting ADCs incorporate the advantages of a modulator in a Nyquist-sampling ADC.

Desired characteristics of adc can be achieve by Figure (1). Here the whole circuit is split into three designs, designing of modulator, designing of 10b cyclic ADC and designing of FIR filter

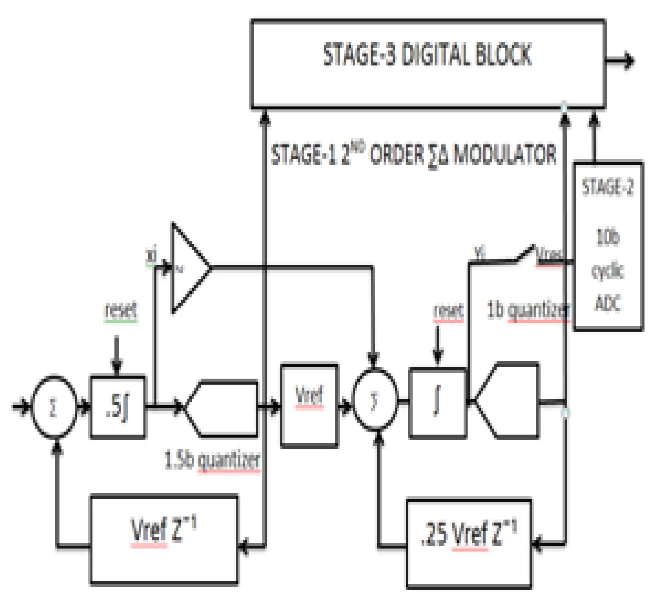

Figure 1: Block diagram of resetting ADC

Stage 1 of the Figure(1) is 2^{nd} order ∑Δ modulator and taken modulator is resetting modulator.

II. RESETTING MODULATOR

To understand 2^{nd} order ∑Δ modulator it is important to understand the working and benefits of 1^{st} order ∑Δ modulator.

Fig. 2 shows an example of a first order resetting ∑ΔADC which is reset after 'N' clock cycles. Since the average of the digital outputs Di(i=1 to N) is the digital estimate of the input Vin the estimate improves as N increases

$$\mathrm{Vin} = \mathrm{Vref} \sum \mathrm{Di}/\mathrm{N} \qquad (1)$$

Resetting modulator architectures for high absolute accuracy, including very high linearity, negligible dc offsetwithhigh OSR have been used for low-frequency (<.5 MHz) or DC input signal applications [14]. Here a resetting ADC with large bandwidth is demonstrated. High bandwidth, low OSR incrementalconverters are analyzed in [10].

A resetting ∑Δ modulator can replace one or more of the front-end stages of a pipeline ADC. Fig. 2 shows an example of a first-order ∑Δ resetting modulator. As with a conventional ∑Δstage, capacitors c1,c2 and the op-amp form an integrator.The input signal is sampled onto capacitor c1 and later integrated onto feedback capacitor c2.In each integrating stepi (i=1 to N) the output of op-amp is quantized to Di by the 1.5 b sub-ADC.

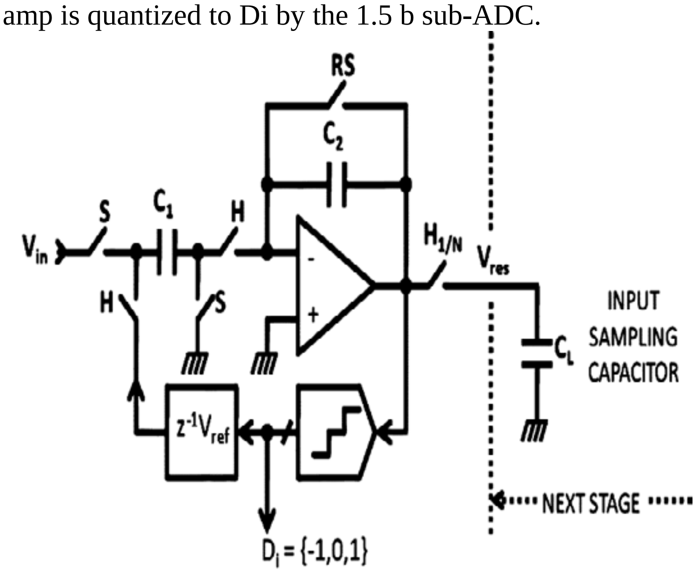

Figure 2: 1^{st} order resetting ∑Δ modulator with OSR=N

Di which has a value -1,0 or 1, ismultiplied byVrefto form the DAC feedback of the ∑Δ modulator. A reset switch across feedback capacitorC2, controlled by clock RS, periodically resets the integrator. In the example shown in Figure (2), clock RS goes high once every N clock cycles, resetting themodulator,and thus this resetting ∑Δ modulator has an OSR of N.

This final integrator output,Vres, is passed onto a load capacitor C_L,before reset, through a switch controlled by clock H1/n.

The load capacitor C_L, is the input sampling capacitor of the next pipeline stage, which quantizes the residueVres of resetting modulator stage.

A good RC-settling match between sampling of the inputsignal onto the capacitors $C_1 – C_4$ and sampling of the input bythe sub-ADC.Without an active front-end S/H, any RC-settlingmismatch between the input signal sampling onto the capacitors C_1 – $C_4$and sub-ADC sampling of the input, can cause an incorrectdecision by the sub-ADC, and this decision error can belarge for a high frequency input signal. To avoid such errorsan active front-end S/H is often used, especially in the case ofhigh-resolution converters.

III. PROPOSED ADC ARCHITECTURE

The proposed architecture (Fig. 1) is a pipeline of a secondorderresetting modulator (stage 1) and a 10 b cyclic ADC

(stage2).While a first-order resetting modulator achieves astage-gain proportional to the number of integrating clock cycles. A second-order resetting modulator isused in stage 1 to achieve a large effective stage-gain inonly five integrating clock cycles. Such a front-end can typicallyreplace the first two stages of a conventional pipeline ADC. Thisfront-end second-order modulator incorporates all the advantagesof a first-order modulator namely,low required op-amp gain, lower settling error, large toleranceof capacitor mismatch, and the elimination of the need for anactive front-end S/H and lower noise due to oversampling.

The front-end modulator samples and modulates theinput at five times the effective conversion-rate. After every five samples, the residue at theoutput of the front-end is passed to the second-stage cyclicADC and the modulator is reset. The cyclic ADC thenquantizes the residue while the front-end processes thenext 5 samples.

IV.CIRCUIT DETAILS

A. FRONT-END MODULATOR

The SC implementation of the second-order resetting front-end (stage 1 of the ADC) is shown in Figure(3).

The first and second integrators are implemented using op-amps A1 and A2 respectively.The outputs of first integrator and second integrator are 1.5 b and 1 b quantized to ai and bi, respectively by thetwo sub-ADCs shown.Both op-amps are implemented as folded cascade OTA.

1. FOLDED CASCADE OTA

For modulator and cyclic ADC we need high gain OTA, So here target design is OTA.Folded Cascode OTA has found a broad use because of itsreduced thermal noise and a possible optimization of power consumption.Folding about the cascode node will increase input and output swing range.For a folded OTA bandwidth performance is high.

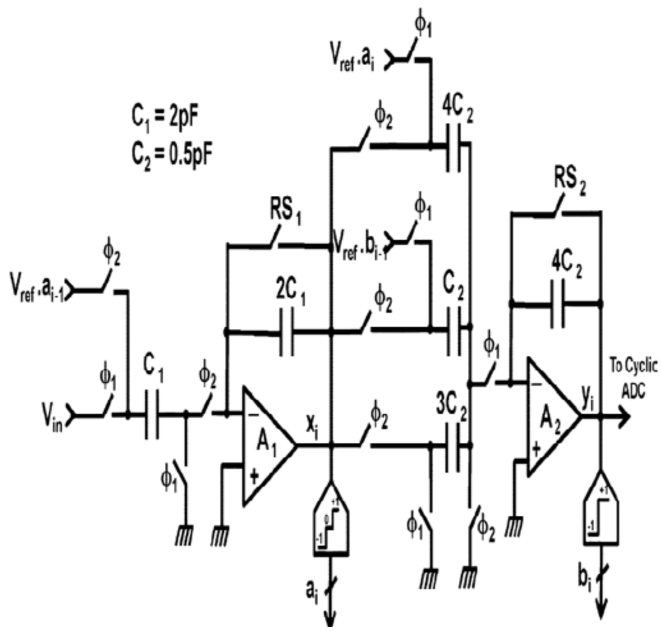

Figure 3: ADC architecture.

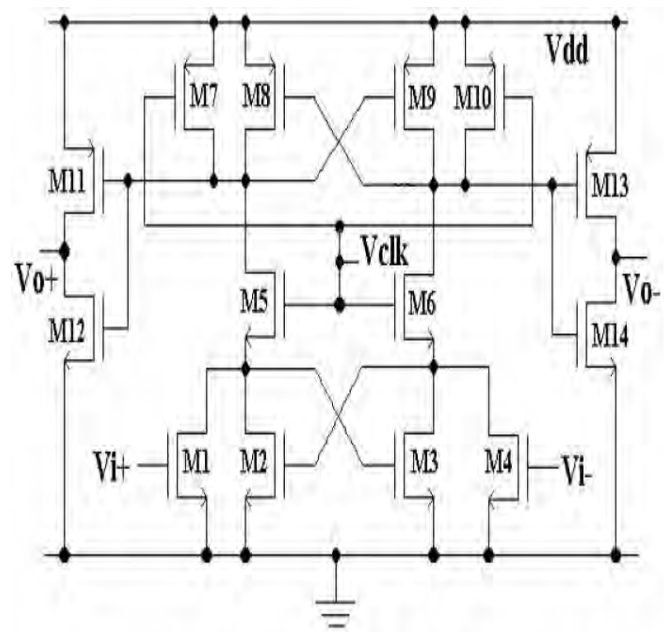

Figure 5: Latched type comparator

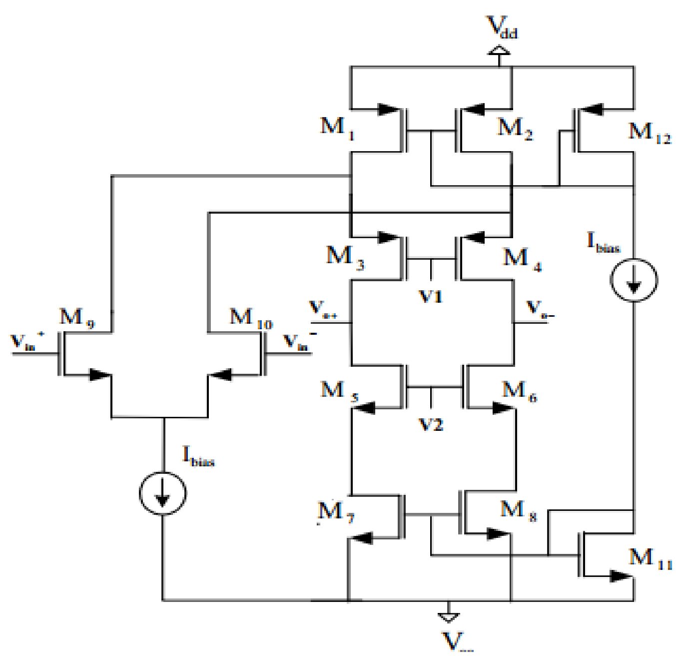

Figure 4: Folded cascade OTA

B. QUANTIZER (1bit and 1.5bit)

Figure 5 shows the 1bit quantizer used in this design. The quantizer consists of a one bit comparator followed by a D flip flop. M1 and M4 are the discharge-current-controllingtransistors which are connected to a feedbacknetwork formed by M2 and M3; M5 and M6 aretransfer gates for strobing; M8 and M9 for another regenerative feedback; M7 and M10 areprecharge transistors; M11-M14 formed twoinverters which act as buffers to isolate the latchfrom the output load and to amplify thecomparator output.

C. D FLIP FLOP

D Flip Flop is presented in theFigure (6). Whenthe clock signal is high the transistors M6and M8 are cut off and the transistors M2 and M4 areturned on.

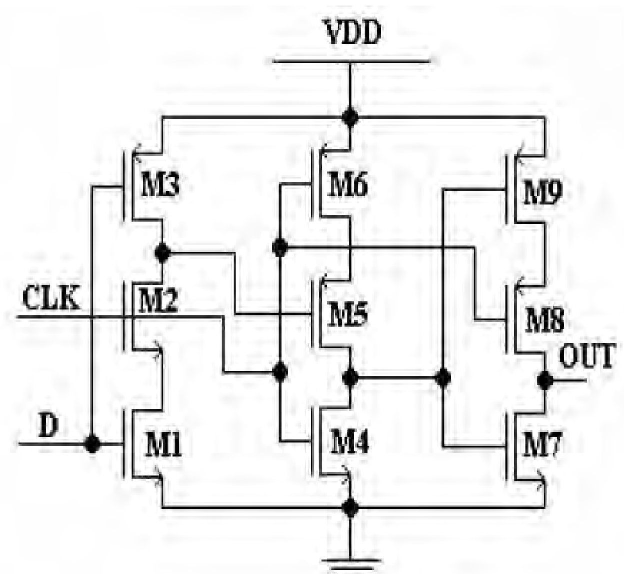

Figure 6: Schematic of D Flip-Flop.

The voltage on M4 drain node is beingpulled to ground and hence forces the transistorM7 cut off. The output node is there for disconnected to either positive rail or the groundand the output therefore is being latched to theprevious value. On the other hand, the transistorsM1-M3 formed a clock-buffered inverter. Whenthe clock signal is high, the drain voltage of thetransistor M2 is the output of this inverter.

Similarly we can also design 1.5bit quantizer as shown in Figure(7).

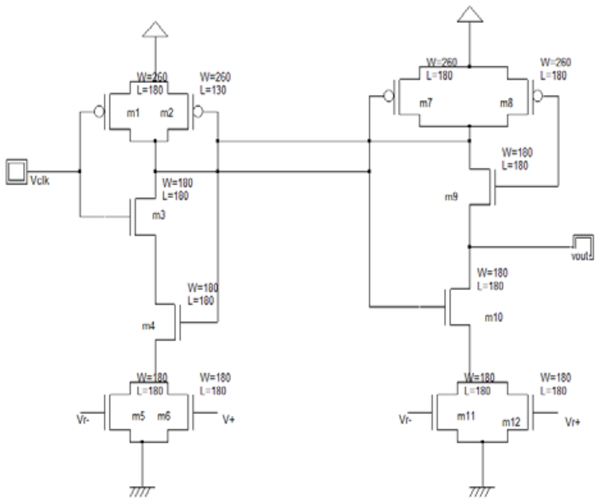

Figure 7: Schematic of 1.5bit Quantizer.

2. CYCLIC ADC

Figure (8)shows the SC implementation of the 10 b cyclic ADC. The cyclic ADC is implemented using a single op-amp. This ADC resolves 1.5b in each half-clock-period to yield 10 b resolution in 5 clock cycles, thus matching the latency of the front-end modulator. The cyclic ADC consumes 8mW.

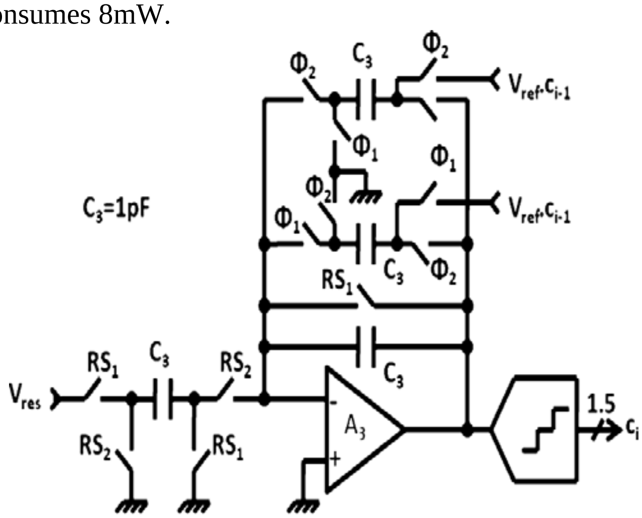

Figure 8: Cyclic ADC

3. DIGITAL FILTER

The digital block, combines the sub-ADC outputs from the second order modulator and the cyclic ADC to give the overall ADC digital output, Dout.The digital block, functions as a linearly-weighted averaging FIR filter.There are several options for choosing the filter such as linearly weighted averaging digital filter, an ideal brick-wall filter,sinc1 filter and a sinc3 filter.

A sinc3 filter, traditionally used in second-order ∑Δ ADCs, has a very good noise decimation factor of 8.9 but suffers from a large worst-case pass-band droop of 11.34 dB, which severely limits the usable bandwidth of the ADC. The simple linearly weighted averaging filter has a relatively poor noise decimation factor of 4.1 but has a low pass-band droop of only 2.77 dB, enhancing the usable bandwidth of the ADC.

Here we are using FIR filter uses feed forward logic. Feed-forward means that there is no feedback of past or future outputs to form the present output, just input related terms. The implementation of an FIR requires three basic building blocksmultiplication, addition, signal delay as shown inFigure (9). Memory also needed to store filter coefficient

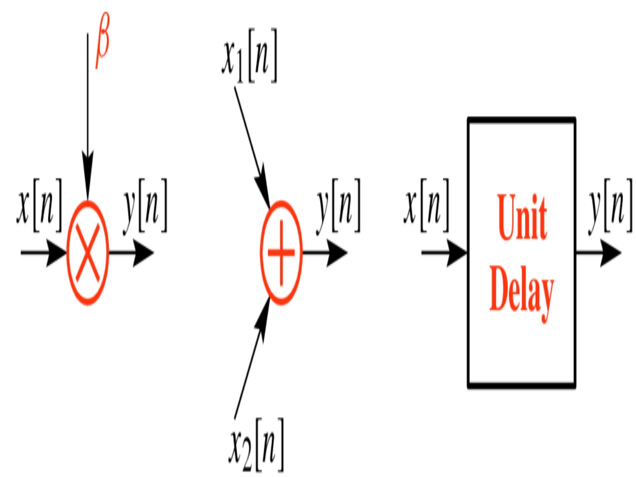

Figure 9: Building blocks of FIR filter.

Block Diagram

Using the building blocks described above, we can construct a block diagram for say an M=3 FIR filter.The signal flow is strictly feed-forward, since all paths connecting the input to the output flow in the forward direction.

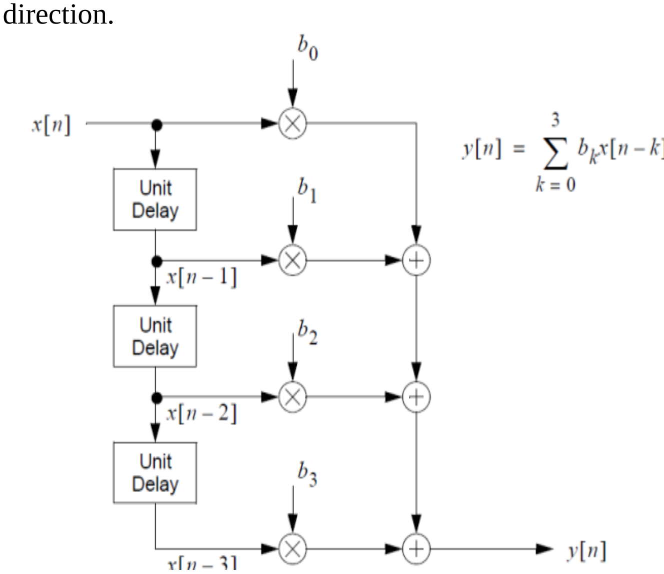

Figure 10: Block diagram of FIR filter.

IV.MEASUREMENT RESULT

Designing of overall circuit in 130nm technology is done

Table 1:Comparative analysis with Lee work

	Lee work	Present work
Resolution	14b	16b
Power	48mW	36μW
Power Supply	2V	1.8V

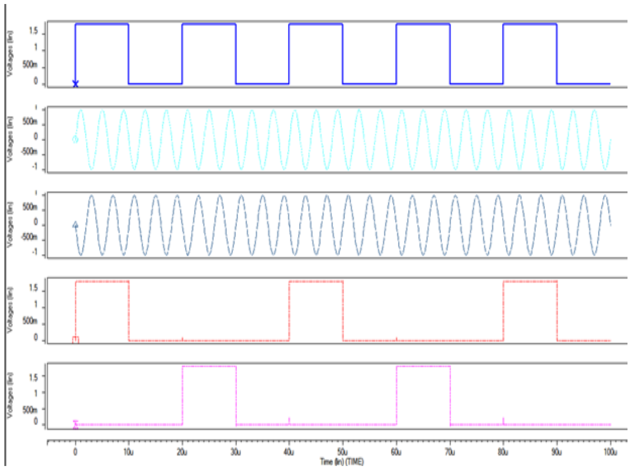

Figure 11: Waveform of 1bit Quantizer

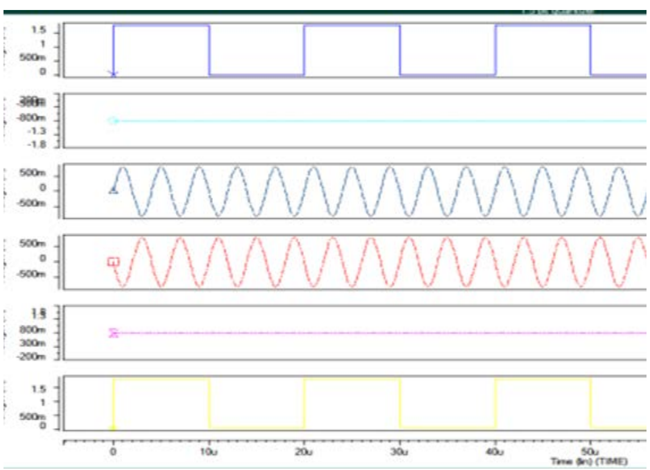

Figure 12: Waveform of 1.5bit Quantizer

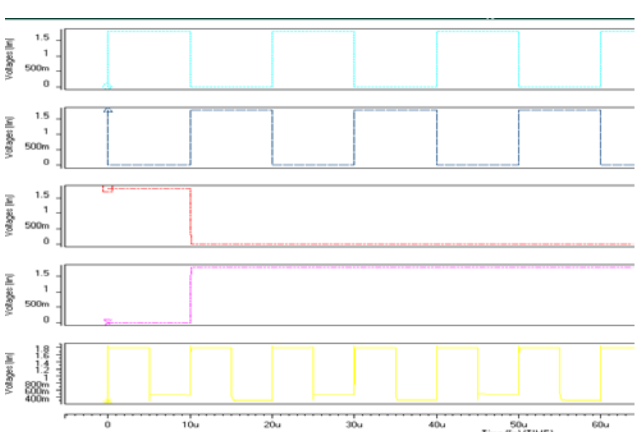

Figure 13: Waveform of Resetting sigma-delta modulator

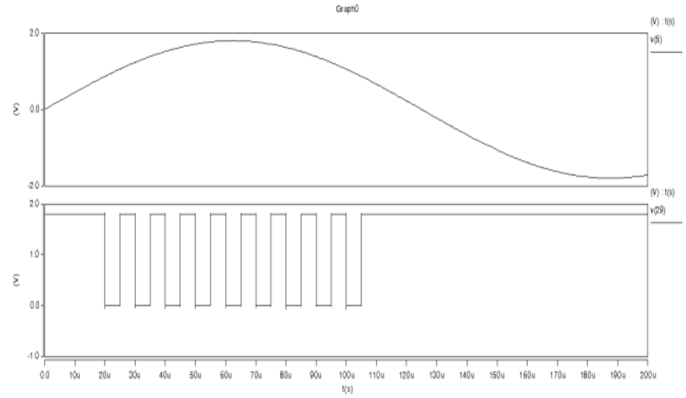

Figure 14: Waveform of Resetting sigma-delta ADC

V. CONCLUSION

This paper proposes a switched capacitor resetting sigma delta modulator in ADC.Explanations are presented about resetting modulator, cyclic ADC and FIR filter.High resolution and power reduction is achieved in 130nm technology.

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