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SIMULATION OF C-OTA FOR LOW POWER APPLICATIONS

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Abstract

The evolution of the microelectronics industry is distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits. The cost of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good design of analogue integrated circuit. To fulfil the above mentioned requirements, the designer must choose the suitable circuit architecture.

This paper presents an optimized methodology to cascode operational transconductance amplifier (C-OTA) design. The challenge in the design of op- amps is the scaling down of the supply voltage and transistor channel length with each generation of CMOS technologies. As CMOS technology continues to evolve, the supply voltages are decreasing while at the same time, the transistor threshold voltages are remaining relatively constant. The decrease in the inherent gain of the nano-CMOS transistors is also of great concern. The design is done for different parameters like gain, bandwidth, phase margin and slew rate etc to optimize MOS transistor sizing. The designed cascode OTA achieves a DC gain of satisfied range and an optimum unity-gain frequency.

Keywords: CMOS IC design, Cascode OTA design methodology, optimization.

Introduction

The evolution of the microelectronics industry is distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits. The cost of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good analogue integrated circuit design. To fulfil the given requirements, the designer must choose the suitable circuit architecture, although different tools partially automating the topology synthesis appeared in the past [1]-[4].The optimization becomes an important method; a heuristic process was developed in [5]. Designing high-performance baseband analog circuits is still a hard task toward reduced supply voltages and increased frequency. The Operational Transconductance Amplifier (OTA) is a basic element in this type of circuit whether switched capacitors technique is kept for ADC design. Our target was to design a cascode OTA circuit insight of Sigma Delta analog-to-digital converter design using for wide band radio applications. This paper is organized as follows. An optimum Architecture of the folded cascode OTA was introduced in section II and its function was analyzed to extract the circuit performances. Section III describes an approach for designing this OTA, clarifies specific design issues, and results. While section IV provides concluding remarks.

OPTIMUM TOPOLOGY C-OTA ARCHITECTURE

Several fundamental issues exist when selecting an optimal architecture for the operational transconductance amplifier. This choice aimed both at large gain and large bandwidth performances. In order to achieve high gain, the differential telescopic topologies can be used. The telescopic architecture is a better candidate for a low power consumption and low noise C-OTA. The performance of simple C-OTA is limited by its input and output voltage swing. To overcome these limits of simple C-OTA and have an

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improved performance a Cascode OTA is used. Although, telescopic OTA has a limited

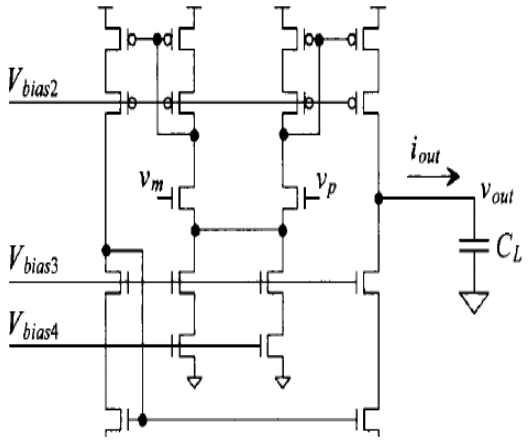

Figure 1:- A cascade OTA circuit (Higher output Resistance)input and output swing.

In order to alleviate some of the drawbacks of telescopic operational amplifier, a folded cascode OTA based on Wilson mirror can be used.

Basic configuration CMOS Cascode OTA

The operational transconductance amplifier (OTA) is used as basic building block in many switched capacitor filters OTA is basically an op-amp without an output buffer and can only drive capacitive loads. An OTA is an amplifier where all nodes are low impedance except the input and output nodes. A useful feature of OTA is that its transconductance can be adjusted by the bias current. Filters made using the OTA can be tuned by changing the bias current Ibias. Two practical concerns when designing an OTA for filter applications are the input signal amplitude and the parasitic input/output capacitances. Large signals cause the OTA gain to become non-linear. The external capacitance should be large compared to the input or output parasitic of the OTA. This limits the maximum frequency of a filter built with an OTA and causes amplitude or phase errors. These errors can usually be reduced with proper selection of Ibias. The performance of simple OTA is limited by its input and output voltage swing. To overcome these limits of simple OTA and have an improved performance a Folded Cascode OTA is used. The name "folded cascode" comes from folding down n-channel cascode active loads of a diff-pair and changing the MOSFETs to p-channels.

The output Voltage of the OTA is given by:

Vout=GmVinRo (1)

The "Unity gain frequency" of the OTA is:

Fu=2πgm/CL (2)

Gm is computed as:

Gm=2πGBWCL (3)

Modeling and Simulation of cascode operational transconductance amplifier at different voltages using AC Analysis:-

Modelling and Simulation of cascode operational transconductance amplifier at 1V using Parameters Analysis:-

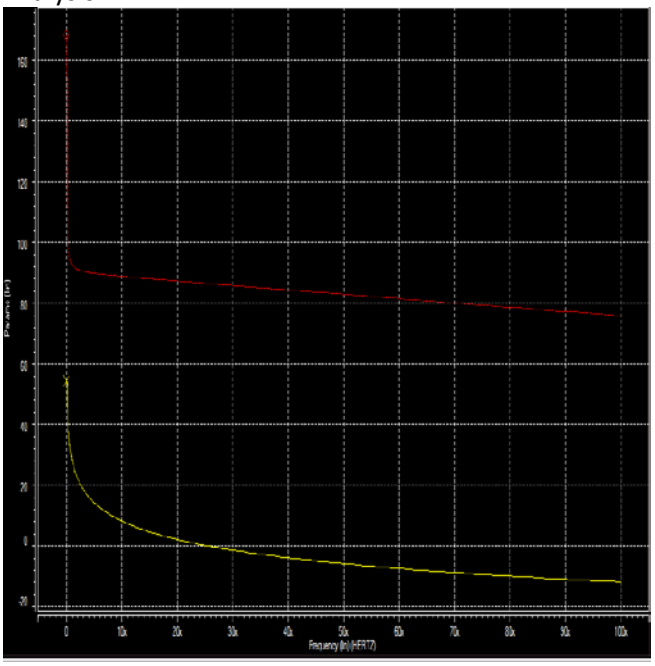

Fig-2. AC Analysis of Cascode OTA

Modelling and Simulation of cascode operational transconductance amplifier at 1V using Transient Analysis:-

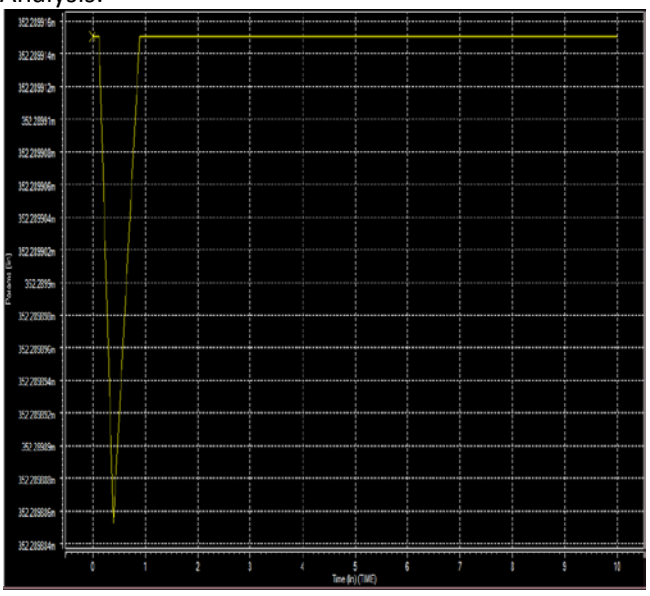

Fig-3:-Transient wave form of Cascode OTA

Modelling and Simulation of cascode operational transconductanse amplifier biasing at 1V using AC Analysis:-

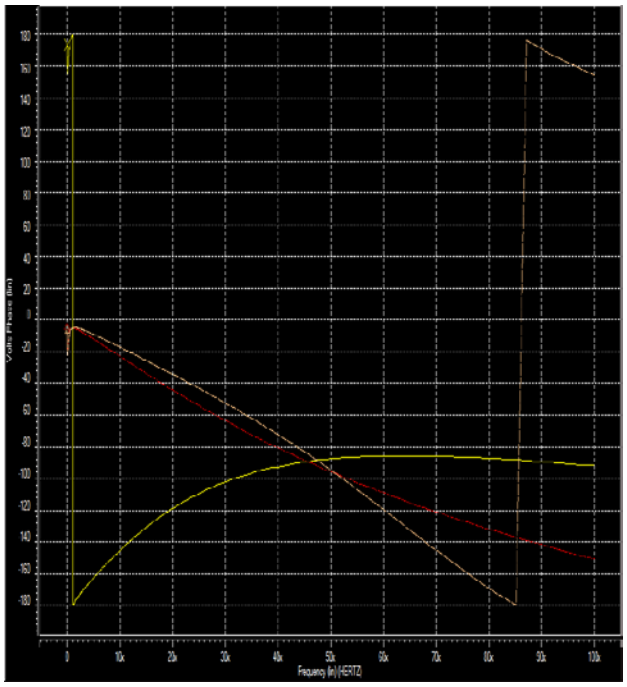

Fig-4:- Biasing of cascade OTA at 1V.

Table 1:- Parameters of OTA

S. No.	Parameter	Value
1	DC Gain in dB	2.4661E+01
2	Band width in GHz	1.6091E+06
3	Phase Margin in degree	9.0558E+01
4	Slew Rate V/µs	2.0285E-05
5	Average Power in µW	1.4908E-04
6	Output Resistance KΩ	5.3949k
7	Unity Gain Frequency in dB	3.0947E+07

Table-2:-Variation of COTA Parameters with Voltage

S. N.	Parameters	0.9V	1.2V	1.4V
1	DC Gain in dB	2.4400E+01	2.4992E+01	2.5065E+01
2	Bandwidth in GHz	1.6076E+06	1.6384E+0	1.7134E+06
3	Phase Margin	9.0700E+01	9.0354E+01	9.0248E+01
4	Slew Rate	1.8112E-05	2.1830E-05	2.3162E-05
5	Average Power	1.2968E-04	1.8739E-04	2.2834E-04
6	Output Resistance	5.5557k	5.1118k	4.8560k
7	Unity Gain Frequency	3.0072E+07	3.2770E+07	3.4659E+07

Results & Discussions:-

The cascode operational transconductance amplifier circuit is design in term of optimum structural device parameters namely bandwidth, output resistance, power etc in addition to the selection of operating supply voltage. By studying the effect of parameter various with supply voltage, V_{DD} as depicted in table 2, it was found that for best performance, the supply voltage must be set around 0.9 V. The lowering of supply supply voltage decreases the power consumption due to proportional scaling but it also affects the circuit slew rate and average power. This is due to lower output swing and pronounced effect of parasitic which deteriorates the bandwidth of the amplifier. As expected, Almost all other parameters improve .

Conclusion:-

Consider a basic CMOS operational transconductanse amplifier with device design parameters set to their default design values especially keeping the minimum length to be greater than twice the diameter for same width as that of a CMOS design. Since below the minimum L, both the gate capacitance and the drive current of CMOS in the middle are smaller in comparison to the seat the edges. This is due to the screening effect produced by adjacent CMOS which proses a maximum limit on the operational transconductanse amplifier for optimal performance. By studying the effect of parameter variations with supply voltage, in Figuer, it was found that for best performance, the supply voltage must be set around 0.9V. The lowering of supply voltage decreases the power consumption due to proportional scaling but it also affects the circuit slew rate and settling time. This is due to lower output swing and pronounced effect of parasitic which deteriorates the bandwidth of the amplifier. As expected, almost all other parameters improve but due to lower swing, robustness deteriorates. The supply voltage must better performance of the cascade operational transconductanse amplifier (OTA) in CMOS technology using Hspice toll simulation. When the variation of the voltage then parameter value are

effected, DC gain & Band width increases, O/P resistance & Power is decreases, Slew rate is varied in the different value of voltage. Hence the minimum supply voltage is better in the Cascode Operational Transconductance amplifier (OTA) in CMOS technology.

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