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Design and Implementation of Thermo Meter code TPG for BIST

K RamaDevi[1], Sarath Chandra Maturi[2]

[1] PG Scholar, Department of ECE, MVSR Engineering College, Hyderabad, India

[2]Associate Professor, Department of ECE, MVSR Engineering College, Hyderabad, India

ramadevi.kothapalli@gmail.com

Abstract

In VLSI Industry testing is an essential process for making the assurance functionality of the chip. This paper is focusing on one of the test methodology called built-in-self-test (BIST).To introduce a novel test pattern generator (TPG) called Johnson counter for test the modules of the chip.TPG is generated here with the re-configurable Johnson counter and a LFSR generated seed values. Bit EX-OR operation is performed between the re-configurable Johnson counter and the seed. The proposed gray counters TPG were produced using Gray counter and Decoder. The Area and power optimization is achieved. We are extended to thermo meter code TPG. The Thermometer codes TPG were produced using the binary counter and binary to thermo meter code converter. The area and speed optimization is achieved. The generated test patterns are given to multiplier circuit. The thermo meter code TPG for producing the test vectors for BIST is coded using VERILOG HDL and simulations, synthesis were performed with Xilinx 13.2 tool.

Keywords: Built-in-self-test (BIST), Test Pattern Generator (TPG), Linear feedback shift registers (LFSR).

Introduction

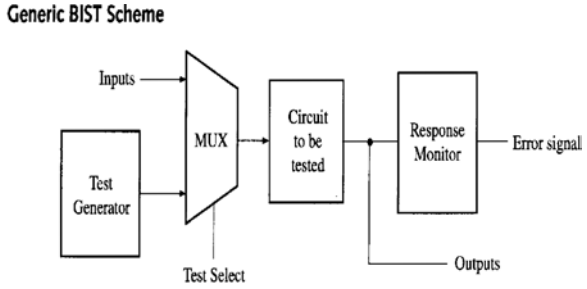
Testing plays a crucial role in any kind of production. The occurrence of imperfection in VLSI circuits results in testing every chip. The possibility of defect might be caused due to various constrains such as malfunctioning of equipments, design errors and material defect. Testing can be performed externally or internally. External testing is performed using automatic test equipment (ATE). The test vectors are generated using ATE and are applied to circuit under test (CUT).The results are analyzed using CAD tools. The drawback of performing testing using ATE is longer time required for testing and high cost of the equipment. Hence there is a shift from external testing to internal testing. Internal testing is performed with the help of built in self test (BIST). BIST reduces difficulty and complexity in testing the circuits. The test vectors generated are applied to the digital circuit andthe circuit response obtained is compared with the true response to determine the fault. For the purpose of pattern generation exhaustive testing or Pseudo exhaustive testing or Pseudorandom testing can be performed. Exhaustive testing applies all possible input combination to the digital circuit.

The advantage of generating test patterns using exhaustive testing is 100% fault coverage. But the drawback is the increased test time. In Pseudo exhaustive testing the circuits are partitioned into small slices and individual slices are tested using exhaustive testing. In Pseudorandom testing the patterns were generated in random fashion. The produced patterns may or may not be repeatable. The Pseudorandom patterns are generated to reduce the test length thereby reducing the time for testing. In traditional techniques the testing vectors were produced using linear feedback shift register [1]. The limitation of generating test vectors is enormous switching operation between the successive test vectors. This frequent change over increases the power requirement. A survey has been performed by P.Girard in [2], on various external testing and internal testing methodologies. A.Abu-Issa and S. Quigley in[3], proposed the architecture to shrink the power dissipation by the process of interchanging the bits to LFSR. The scan chains are ordered initially. The test vectors were utilized by the scan chains and then the reordering process is carried out to improve the correlation among the test vectors. P.Girardet.al in [4], used simulated annealing algorithm to curtail the

Corresponding author: K RamaDevi

energy.S.Wang and S.Gupta in [5], used two LFSR operating at varying speed to shrink the unwanted transitions. F.Corno et.al developed a test pattern generator for shrinking the powernecessary in combinational circuits [6]. P.Girard et.al in [7], adjusted the clock pulse for decreasing the power. Instead of applying single clock pulse two separate clock pulses were produced. D. Gizopoulos et.al in [8] proposed a methodology to produce deterministic patterns for testing data paths.

II BIST ARCHITECTURE



BIST Controller Unit (BCU): It controls the test execution, manages TPG, ORA and the Multiplexer.

Test Pattern Generator (TPG): It generates the test pattern for the CUT, The patterns may be generated in pseudorandom.

Circuit Under Test (CUT): It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory.

Output Response Analysis (ORA): It analyses the CUT output with the expected output, if both are same error signal is low if not error signal is high.

MUX: If test select is high test generator outputs are given to CUT, If test select is low normal inputs are given to CUT.

III TPG using Reconfigurable Johnson counter and LFSR

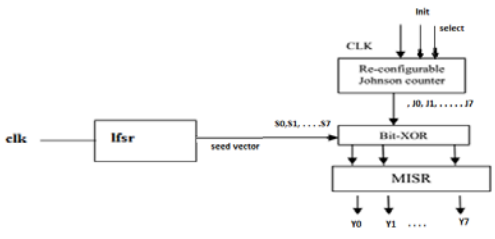


Figure 1: TPG using reconfigarable jhonson counter

Test Pattern Generator contains the three operational blocks for generating the TPG. Those are

1. Reconfigurable Johnson counter
2. Seed generation using LFSR
3. Bit EXOR operation
4. MISR

Re-configurable Johnson counter

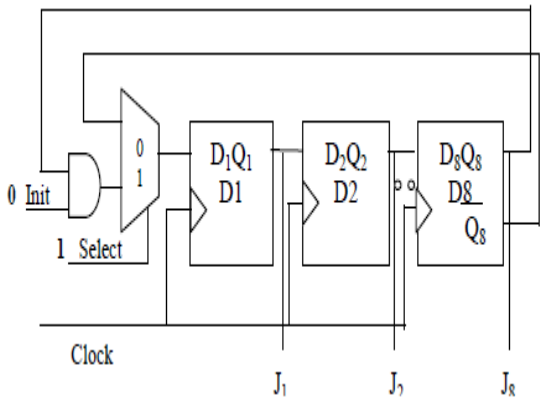


Figure 2: Intialization mode

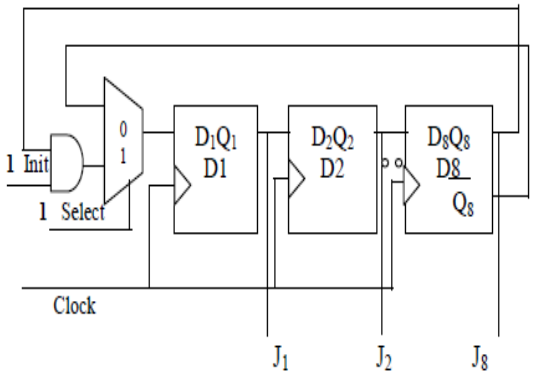


Figure 3: Circular shift mode

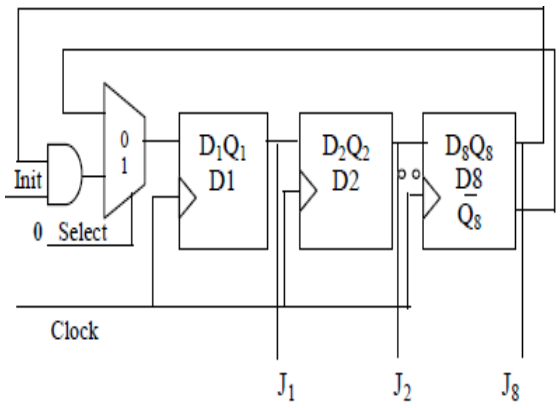


Figure 4: Normal mode

The Johnson vectors were produced by utilizing reconfigurable Johnson counter.reconfigurable Johnson counter is constructed with the help of an AND gate, Multiplexer and eight Delay flip-flops are connected together to store the bits. Johnson vector were made to operateInitialization mode, Circular shift mode and normal mode toinitialize the flip flops the select input of the multiplexerassigned with the value 1 and one of the inputs to the and gate is assigned with the value 0 the clock signal is applied to initialize the registers. The initialization operation of the Reconfigurable Johnson counter. The circular shift mode performs shifting operation and the output q8 of d8 register is feedback. To perform circular shift operation the select input of the multiplexer is choosen to be1 and input to the AND gate init is assigned with the value 1 the clock input is clocked to operate Johnson counter in circular mode.While operating in normal mode the inverted bit corresponding to last flip flop is feedback as shown in Fig 4.

Seed generation using LFSR

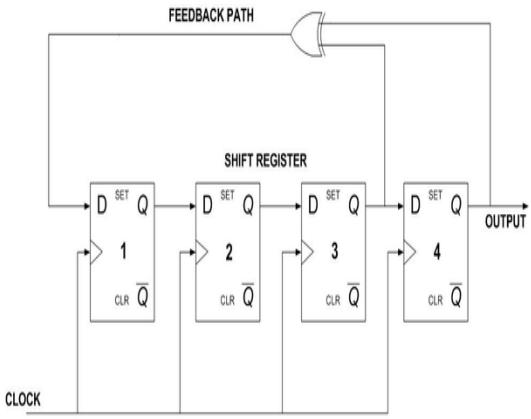
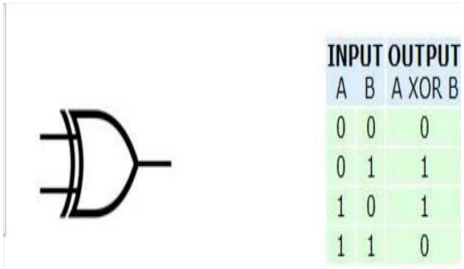


Figure 5: LFSR

Xorgate



INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Figure 6:logic symbol and truth table of XOR gate

MISR

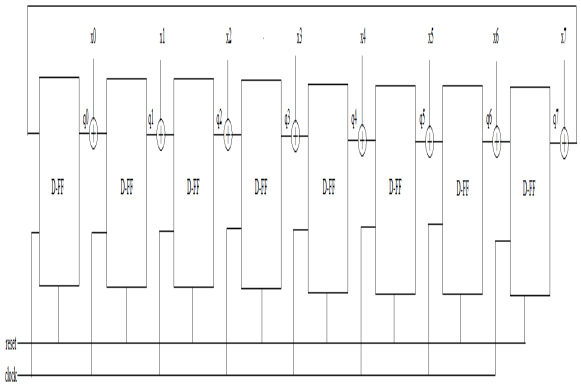


Figure 7:Block diagram of MISR

IV TPG using gray counter

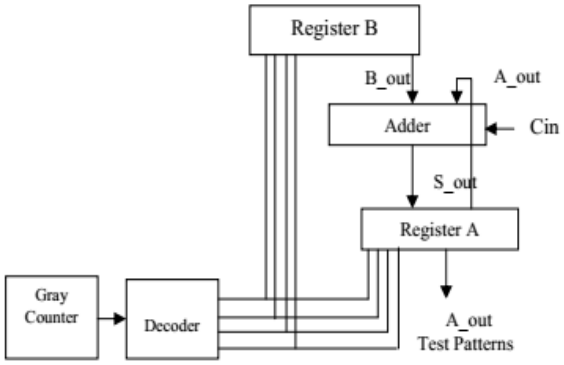


Fig 8: TPG using gray counter

The demand for the portable devices is increasing tremendously. So Area and Power optimization are essential to satisfy the demands of the consumer. The patterns generated using Existing methodology finds complexity inArea and Power. For the purpose of optimization the patternswere generated using Gray code counter. The purpose of choosing gray code counter is to reduce the power requirements. The gray code counters prevent the unwanted signal transition at the input. The input bits vary in single bit position. For every rising edge of the clock four bit gray code results were applied to 3 to 8 Decoder circuit. The results of decoder circuit were applied to the adder circuit through Register B. The set reset flip flop is used as Register A to store the computed result. The patterns were obtained through register A. The patterns produced were tested on Multiplier circuit. The response obtained is compared with the

forecasted result to verify the exact functioning of the circuit.

Binary to gray code conversion

Binary to gray code conversion is a very simple process. There are several steps to do this types of conversions. Steps given below elaborate on the idea on this type of conversion. (1) The M.S.B. of the gray code will be exactly equal to the first bit of the given binary number. (2) Now the second bit of the code will be exclusive-or of the first and second bit of the given binary number, i.e. if both the bits are same the result will be 0 and if they are different the result will be 1. (3)The third bit of gray code will be equal to the exclusive-or of the second and third bit of the given binary number. Thus the **Binary to gray code conversion** goes on. One example givenbelow can make your idea clear on this type of conversion.

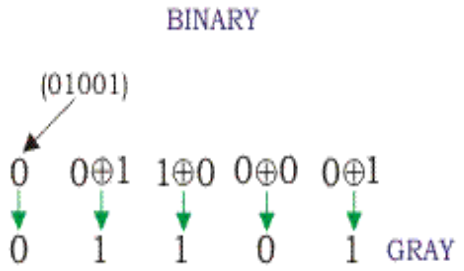


Figure 9:Binary to gray conversion

Thus the equivalent gray code is 01101. Now concentrate on the example where the M.S.B. of the binary is 0 so for it will be 0 for the most significant gray bit. Next, the XOR of the first and the second bit is done. The bits are different so that resultant gray bit will be 1. Again move to the next step, XOR of second and third bit is again 1 as they are different. Next, XOR of third and fourth bit is 0 as both the bits are same. Lastly the XOR of fourth and fifth bit is 1 as they are different. That is how the result of binary to gray code conversion of 01001 is done whose equivalent gray code is 01101.

Decoders:

A decoder is a combinational circuit that converts coded inputs to another coded output. The famous examples of decoders are binary n-to-2n decoders and seven-segment decoders. A binary decoder has n inputs and a maximum of 2n outputs. As we know, an n-bit binary number provides 2n

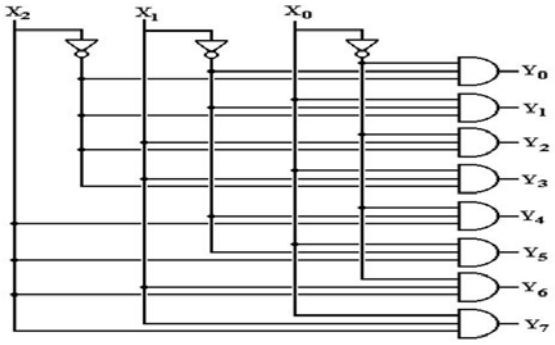


Figure10: Logic Diagram of decoder

Ripple carry adder circuit.

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Circuit diagram of a 4-bit ripple carry adder is shown below.

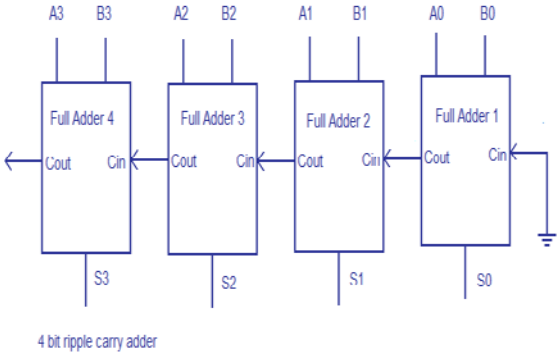


Figure11: Ripple carry adder

Sum out S0 and carry out Cout of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the same way, Sum out S3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propagation delays of all full adder circuits inside it.

V.Thermo meter code TPG

Three bit binary up down counter is used. The results of binary counter are converted into thermometer code using binary to thermometer code converter. The eight bit results produced from binary to thermometer code converter were given to adder through Register B and Register A The set reset flip flop is used as Register A. Finally the 4 bit test patterns is generated. These patterns are tested on multiplier circuits

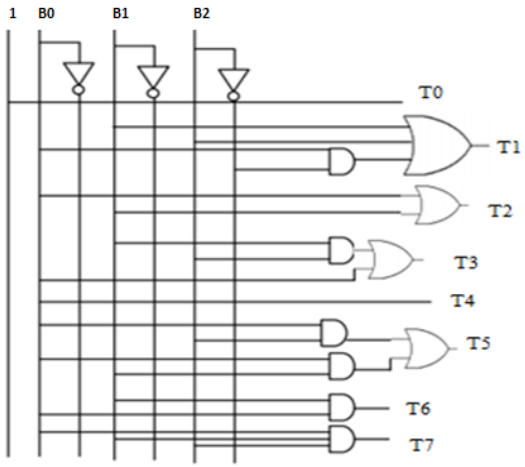


Figure12:Logic diagram of binary to thermometer code converter

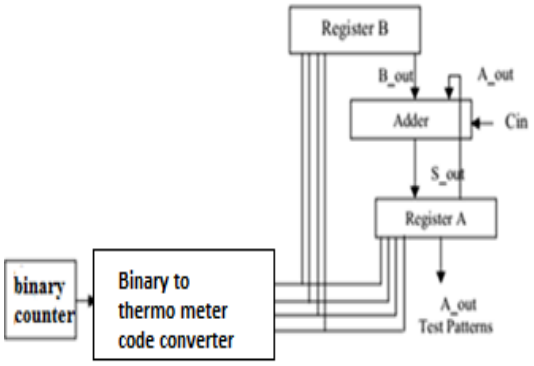


Figure 13: Block diagram of thermometer TPG

CUT -Design of Multiplier

Multipliers are widely used in DSP operations such as convolution for filtering, correlation and filter banks for multirate signal processing. Without multipliers, no computations can be done in DSP applications. Multipliers are one the mostimportant component of many systems. So we always need to find a better solution in case of multipliers. Our multipliers should always consume less power and cover less Area. For that reason, multipliers are chosen for testing in our proposeddesign. We are going to implement 4x4 multiplier by taking corresponding input from the 4bit test pattern generators.

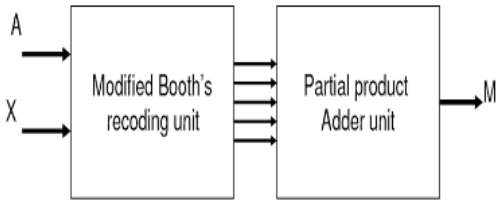


Figure 14: Block diagram of multiplier

Modified Booth's Recoding Unit Radix 2 Method

Here, we have this recoding unit using multiplexers. Select lines to multiplexer are input bit sequence of multiplier and outputs are according to modified table given in table1. So, in this scheme, partial products are always one bit more than input vector. If our multiplier is of n bit then partial products are always n+1.

Table 1: Modified Booth's Recoding table

MODIFIED BOOTH'S RECODING TABLE FOR RADIX 2

X_i	X_{i-1}	Y	Partial Product Explanation
0	0	0	All 0's
0	1	1.A	$[A_{(n-1)}, A]$
1	0	-1.A	$[A_{(n-1)}, (-A)]$
1	1	0	All 0's

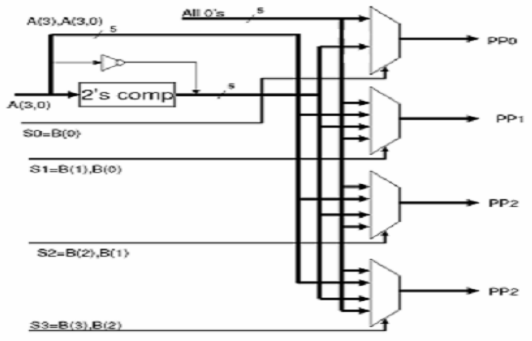


Figure 15: Architecture of Booth's recoding unit radix 2

In this architecture, select lines for multiplexers are multiplier input bits taken according to recoding scheme given in table. Which are similar to General Booth's recoding scheme. We have used 4

multiplexer out of which 3 are 4x1 and one is 2x1.Each input vector is of n+1 of input bits of multiplier. 0^{th} and3rd input vector are always zero and 1stposition input vector is multiplier input (A) appended with extra zero at MSB to increase its width to n+1, it does not change original value. 2nd position input vector is taken 2's complement of input (A) with appending inverted MSB bit of input vector. This architecture generates four partial products vector according to table .

Modified Partial Product Adder

The partial product obtained from Booth's recoding unit needs to be added properly to get correct output of a multiplication. The addition scheme of partial product is same as Browns array multiplier except for MSBs. MSBs of partial products need to be added carefully. For that, new structure of an adder array is proposed. This modification removes the problem of large number of correction bits, which in turn require more number of adders. The proposed partial product adder arrays for 4 bit input sequence using radix 2 algorithms.

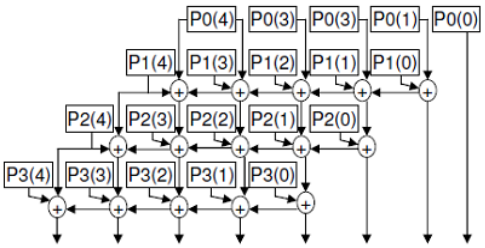


Figure 16: Partial product adder unit for radix 2 recoding of 4 bit input

VI.SIMULATION RESULTS

The various design of the test pattern generation for BIST is implemented using Xilinx ISE 13.2 software. The design is coded in Verilog HDL and simulations were performed using Xlinx 13.2 software. The test patterns generated were tested on 4*4 Multiplier circuit. The analysis of area and power are performed using Xilinx ISE 13.2 software.

A)Johnson Counter TPG

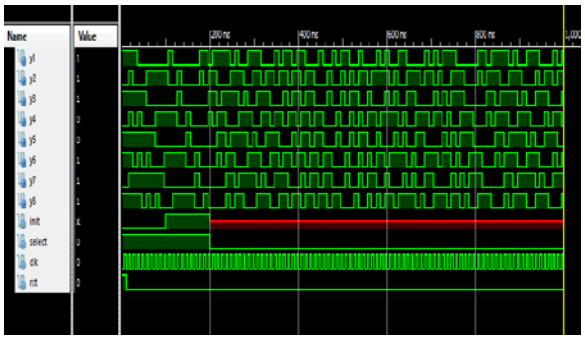


Figure 17: Test pattern generation using Johnson counter

B)Gray Counter TPG

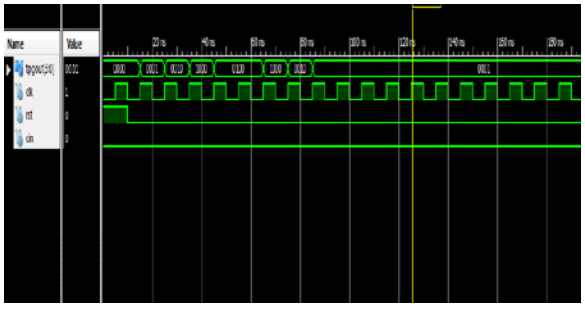


Figure 18: TPG using Graycounter,decoder and accumulator

C)Thermo meter code TPG

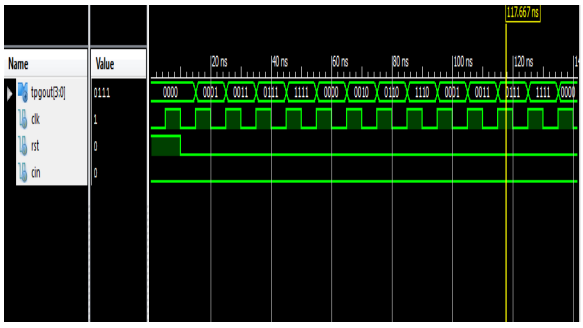


Figure 19 TPG using binary to thermo meter code converter

D)Testing of Multiplier Using TPG

The faults were injected into the multiplier circuit. Fig shows testing of multiplier circuit. The expected result is computed by the signal p1.The predicted result is computed by the signal golden signature The expected result is compared with the predicted result to verify whether the fault is identified by the test pattern.

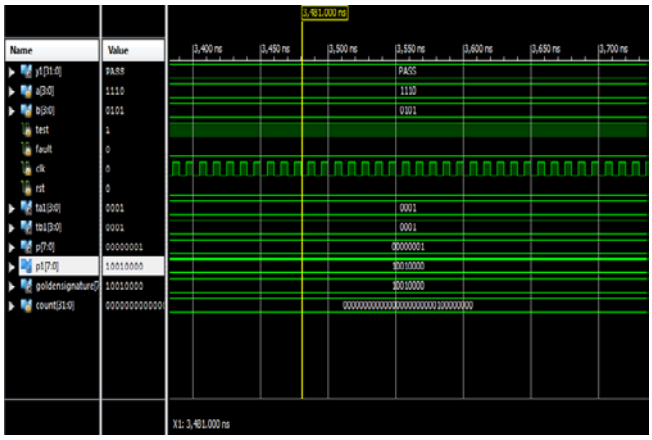


Figure20: Testing of multiplier using thermo meter code TPG

E)Comparision of various TPG'S

Table 2: Comparison of various TPG'S

VARIOUS TPG'S	AREA	DELAY (ns)	POWER (W)
RECONFIGARABLEJHONSON COUNTER	13	3.437	0.109
GRAY COUNTER	10	3.449	0.084
BINARY TO THERMO METER CODE CONVERTER	7	2.731	0.096

VII CONCLUSION

The architecture has been proposed to generate the test patterns for BIST. Power and area optimization is achieved by generating patterns using gray counter TPG. Area and delay optimization is achieved by generating patterns using thermo meter code TPG Johnson counter, Gray counter, thermo meter code TPG are simulated and synthesized by using Xilinx 13.2 tool

REFRENCES

1. Y. Zorian, "A distributed BIST control scheme for complex VLSI devices," in *11th Annu. IEEE VLSI Test Symp. Dig.Papers,*Apr.1993,pp.4–9.
2. P. Girard, "Survey of low-power testing of VLSI circuits,"*IEEE Design Test Comput.*, vol. 19, no. 3, pp. 80–90, May–Jun.2002.
3. A. Abu-Issa and S. Quigley, "Bit-swapping LFSR and scan chain ordering: A novel technique for peak- and average power reduction in scan-based BIST," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 28, no. 5, pp. 755–759,May2009.
4. P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, "Low-energy BIST design: Impact of the LFSR TPG parameters on the weighted switching activity," in*Proc. IEEE Int. Symp.Circuits Syst.*, vol. 1. Jul. 1999, pp. 110–113.
5. S. Wang and S. Gupta, "DS-LFSR: A BIST TPG for low switching activity," *IEEE Trans. Comput.-Aided DesignIntegr. Circuits Syst.*, vol. 21, no. 7, pp. 842–851, Jul. 2002.
6. F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M.Violante, "Low power BIST via non-linear hybrid cellular automata," in *Proc. 18th IEEE VLSI Test Symp.*, Apr.–May2000,pp.29–34.
7. P.Girard, L.Guiller,C. Landrault, S. Pravossoudovitch, and H.Wunderlich, "A modified clock scheme for a low power BIST test pattern generator," in *Proc. 19th IEEE VTSVLSITestSymp.*Mar.–Apr.2001,pp.306–311.
8. D.Gizopoulos, N. Krantitis, A. Paschalis,M. Psarakis, and Y.Zorian, "Low power/energy BIST scheme for datapaths,"in *Proc. 18th IEEE VLSI Test Symp.*, Apr.–May 2000, pp. 23–28.
9. Y. Bonhomie, P. Girard, L. Guiller, C.Landrault, and S. Pravossoudovitch, "A gated clock scheme for low powerscan testing of logic ICs or embedded cores," in *Proc.10thAsian TestSymp.*,Nov.2001,pp.253–258.
10. C. Laoudias and D. Nikolos, "A new test pattern generator for high defect coverage in a BIST environment," in *Proc.14thACM Great Lakes Symp.VLSI*, Apr. 2004, pp. 417–420.

Author Details:

	**K. RamaDevi**has completed her B.tech in Electronics and Communication Engineering from TKR College of Engineering and Technology, J.N.T.U.H Affiliated College in 2013. She is pursuing her M.E in Embedded Systems and VLSI Design from MVSR Engineering College, O.U Affiliated College.
	**Sarath Chandra Maturi** is an Assistant Professor at MVSR Engineering College, Hyderabad in ECE Department. He received his B.Tech degree in Electronics and Communication Engineering from Vel'sSrinivasa College of Engineering and Technology, Chennai, and M.E degree in Embedded Systems and VLSI design from MVSR Engineering College, Hyderabad. His research interest is Low power VLSI design.