ISSN: 2348 - 2117

International Journal of Engineering Technology and Computer Research (IJETCR)
Available Online at www.ijetcr.org
Volume 3; Issue 3; May-June; Page No. 09-13

Design & Simulation of MQAM Based Zigbee Transreceiver Using Verilog

Vaishali Patil[1], Prof. Mithilesh Mahendra[2], Prof. Parag Jawarkar[3]

[1]Nagpur University, Department Of Electronics & Comm., Abha Gaikwad-Patil College of Engg., Nagpur,India

Patil.vaishali87@gmail.com

[2]Department of Electronics & Comm., Nagpur University, Abha Gaikwad-Patil College Of Engg., Nagpur,India

mithileshmahendra@gmail.com

[3] Department of Electronics & Comm., Nagpur University, Abha Gaikwad-Patil College of Engg., Nagpur,India

jawarkar@gmail.com

Abstract:
Digital MQAM Transceiver was enforced on FPGA for low price, low power and easy wireless Communication like zigbee The MQAM Transceiver primarily Transmit and receives on a 2.4 GHz band. The Transceiver encompass chip generator, up-sampler, FIR filter, PISO (parallel in serial out), SIPO (serial in parallel out), FIR filter, down-sampler and chip-decoder blocks. These blocks area unit designed using Verilog in Xilinx ISE 13.1 then enforced on Spartan 3 XC3S200E FPGA. Here to verify the practicality of receiver block the measurement & simulation results are also presented.

Key Words: Zigbee, FPGA, MQAM, HDL, Verilog.

INTRODUCTION:

Current millennium has seen explosive growth in wireless communication. The short vary wireless communication has been used for accessing networks and services while not cables, that may be fast-growing technology for providing flexibility and quality. Major advantages of the technology includes the low value, dynamic network formation, and easy of preparation [1, 2]. There are totally different protocol standards used for wireless communication having short range namely the Bluetooth [3], ZigBee [4] and Wi-Fi [5]. Among these standards ZigBee over IEEE 802.15.4 protocol will satisfy a wider style of industrial desires because of its semi permanent battery operation, wider useful range and reliableness of the mesh networking design [6]. Wireless Personal Area Networks (WPANs) and ZigBee are accustomed transfer short messages like commands of information over a brief distance. Like WPAN, ZigBee wants little infrastructure for data exchange. This feature permits the ZigBee alliance cluster for tiny, power-efficient and inexpensive solutions to implement during a wide selection of wireless devices. Thus ZigBee alliance cluster along side IEEE 802.15.4 standard forms the ZigBee protocol networking layers for low data rate short range wireless communication. This standard provides (MAC) medium access control and (PHY) Physical layer specifications for low rate wireless connection for fixed, moveable and moving devices with restricted battery power consumption. Low battery power consumption is biggest advantage of the standard as a result of the actual fact that, most of time the network devices are in sleep mode.

1. LITRATURE ANALYSIS:

Zigbee layers square measure supported reference model of the (OSI) Open Source Interconnect. Ripping a network protocol into layers has further benefits. In zigbee protocols the lower layers are often obtained from a third party and are independent of the application, therefore all got to do is to create alterations within the application layer. Zigbee standard describes only the protection layers, networking and application of the protocol and adopts MAC layers and IEEE 802.15.4 PHY as part of Zigbee networking protocol. The advantage of custom proprietary application/networking layers is that the memory footprint of smaller size needed to implement entire protocol which results within the reduction in price.

For acknowledgement frame,The Zigbee digital transmitter has enforced and designed by Rafidah Ahmad et al. [7]. A Verilog HDL is used to model transmitter so this design is implemented over Spartan-3E FPGA. The

Corresponding author: Vaishali Patil

digital transmitter comprised of symbol to Cyclic Redundancy Check (CRC) block , Chip block, Bit to symbol block and OQPSK modulator and logic analyzer and pattern generator. By using Verilog, it gives improvement of improvement of 35% in range of slices used,11% in Flip flops used, 92% in range of multiplexers used and improvement of 30% in LUT's used.

Another Zigbee transmitter using VHDL by Rahmani [8] has designed enforced on Spartan-2 board. The transmitter design consists of symbol-to-chip block, bit-to-symbol block and OQPSK modulator. In line with the IEEE 802.15.4 PHY economical generation of the transmit signal can be achieved by using single step VCO modulation transmitter topologies or I/Q conversion. From VHDL source net list was created and for Synthesis Synplify professional synthesis tool was used. This transmitter was then tested on-board. These two papers show that VHDL module needs an additional number of slices. Therefore, it results in terribly large design size.

The Zigbee transmitter's digital part is designed either with VHDL or Matlab, schematic. The transmitter was designed and simulated by Shuaib et al. [9] using Simulink/Matlab and its performance was evaluated. DSSS spreading techniques utilized by Zigbee in PHY layer to cut back influence of noise from neighboring network and increase its power. For 2.4GHz band OQPSK technique used for chip modulation. Fifteen bit PN chip sequence is employed to map every 4 bit symbol. In 868 MHz and 915 MHz bands one-bit symbol is mapped using BPSK modulation. The relocation among the available spectrum is created potential by having many frequency bands. The access to the communicating is controlled by MAC layer. Through acknowledgements and retransmission, it provides flow control. Using Simulink/Matlab, 3 models for 3 Zigbee bands physical layer are designed. However, because of involvement of additional logic functionality, for big styles schematic approach is inappropriate.

From the above survey, we will simply explore that using Schematic, Simulink/ Matlab and also using VHDL, many researchers have designed the Zigbee transmitter, and implemented through Spartan and Virtex development board. None of the transmitter using Verilog is intended, which uses lesser LUTs, range of slices, etc. Using totally different methodologies like schematic, Matlab, and VHDL, various studies designed digital receivers. However, once the circuit is advanced Schematic approach isn't sensible as a result of a protracted style timeframe is needed by technique and Matlab will solely be used for simulation and modeling. Behavioral modeling of digital style goes through HDL, that is additional time-efficient than different methods. Most significant the HDL code may be enforced and simulated directly on FPGA as a prototyping device, or on an ASIC.

2. QUADRATURE AMPLITUDE MODULATION:

QAM systems are widely used in trendy communication systems where most output is required beneath minimum bandwidth condition, thus being considered another approach of fast spectral efficiency in optical communications. Futhermore, the benefits of MQAM have been wide accepted for microwave digital radio applications and voice band modems, along side Digital Video broadcasting-cable (DVB-C), in addition to wireless communications for the military [10].

In general terms ,QAM will be outlined because the digital modulation format wherever data is sent within the amplitude and phase of a carrier signal .This scheme combines two carriers whose amplitude are modulated with same optical frequency and with regard to one another phases are shifted by 90 degrees with regard to one another. These carriers are known as (I) in phase carriers and (Q) quadrature-phase carriers.

An M-ary quadrature amplitude modulation (MQAM) signal can be defined by the subsequent equation:

$$S_m(t) = A_m .g(t). \cos(2\Pi f_c.t + \Theta_m)$$

$$m=1, 2,\ldots., M \qquad \ldots (1)$$

Where, Sm(t) represents the bandpass signal chosen from the M Possible waveforms ,fc symbolizes the carrie frequency. The g(t) is signal pulse with a real value whose shape effects the spectrum of the transmitted signal. Am and Θm denotes the amplitude and amplitude and phase angle of the Mth symbol, given by

$$A_m = \sqrt{(A_m^I)^2+(A_m^Q)^2}$$

$$\Theta_m = \tan^{-1}(A_m^Q / A_m^I)$$

Where, m=1,2,…..,M … (2)

In these equations, Am I and Am Q € { 1±d, 2±d ,3±d,..,(M-1)d} indicate the I and Q amplitudes corresponding to possible M symbols in two dimensional space and d is the constant whose value is determined by the average transmitted power. Otherwise, the band pass QAM signal in (1) can be represented equivalently in terms of its quadrature components and phase as follows:

$$S_m(t) = A_m^I . g(t).\cos(2\Pi f_c.t) - A_m^Q . g(t).\sin(2\Pi f_c.t)$$

Where,

m=1, 2,.., M …(3)

The transmitted bandpass signal s(t) , which contains all the symbols represented by possible M signaling Waveforms for QAM, can be expressed as [11].

$$S(t) = \mathrm{Re}\{(\sum I_n . g(t - nTs) . e^{j2\Pi fct})\} \quad \ldots(4)$$

Where, Ts refers to the symbol duration, (Rs =1/Ts indicates the transmission rate in symbol/second) and {In} represents the discrete information-bearing sequence of symbols and is complex value for QAM.

3. TRANSCEIVER ARCHITECTURE:

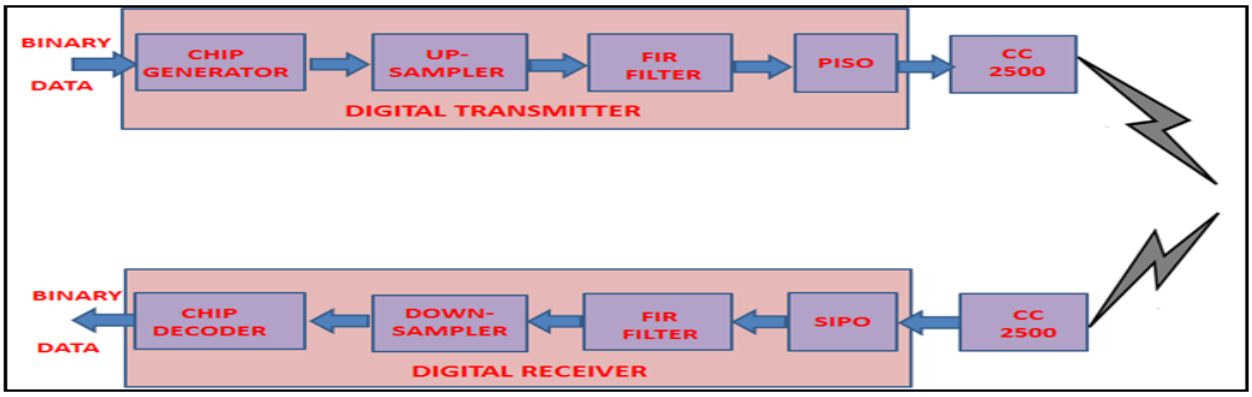

Figure 1: Block diagram of zigbee transceiver

For 2.4 GHz band zigbee applications, sixteen channels are accessible with 5 MHz sample channel spacing .The Transceiver design is shown in fig.1. The binary data is first applied to chip generation block that first maps every four bits into one symbol. Then every symbol is mapped into eight bit p-n chip sequence. Afterward every little bit of p-n sequence is up sampled to match nyquist criteria. The even bits are up sampled by “up sampler-I”, and odd bits are up sampled by “up sampler- Q”. These up sampled bits area unit suffered separate Fir filters. The output of up sampler-I is suffered filter Fir-I and output of up sampler-Q is suffered filter Fir-Q. These filters area unit nothing however [*fr1] trigonometric function pulse shaping filter’s that is reduces the digital noise.

The output of FIR is 10bit block that is then transmitted to “CC2500” module serially by parallel in serial out (PISO) block.“CC2500” module transmits incoming packets to wireless channel.

At receiver facet “CC2500” receiver module receives the packets serially & serial in parallel out (SIPO) converts the serial packets into parallel blocks. These parallel packets area unit the applied to FIR filter. The output of FIR filter is then down sampled by down sampler. The output of down sampler is that the applied to chip decoder. The chip decoder decodes incoming chip signal and at output provides corresponding four bit symbol. This data is then applied to parallel to serial device which provides serial stream of original binary data sent by transmitter.

4. RESULT AND DISCUSSION:

A. Simulation Waveforms:-

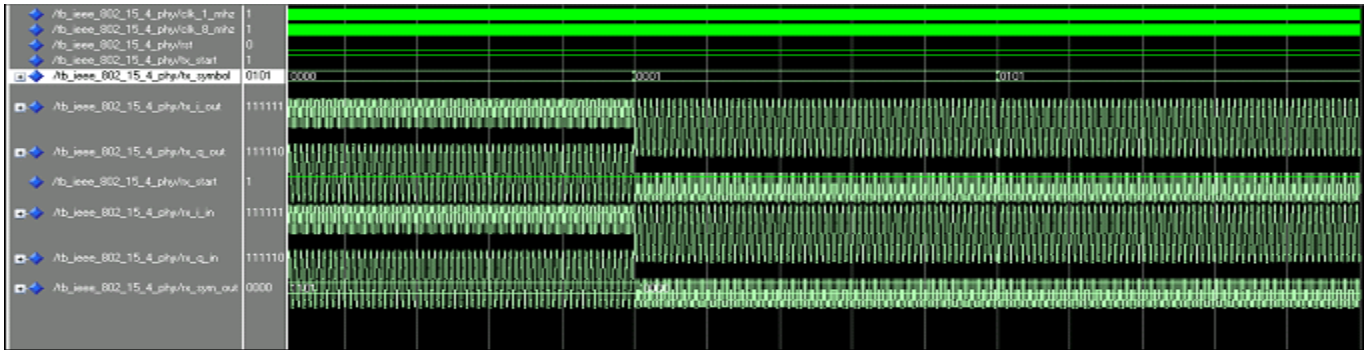

Figure 2: Output Simulation Waveform on Modelsim 6.2 C simulator

The simulation waveform zigbee transceiver is shown in Fig.2. For various symbols modulated I-channel & Q-channel and demodulated I-channel & Q-channel waveforms are shown in figure. For simulation Mentor Graphics "modelsim 6.2 C" tool is employed. Then to "reset" bit negative edge trigger is applied. The Logic high is applied to the "start" little bit of transmitter and 1 MHz & 8 MHz clocks are applied to transmitter.

A. RTL Schematic :

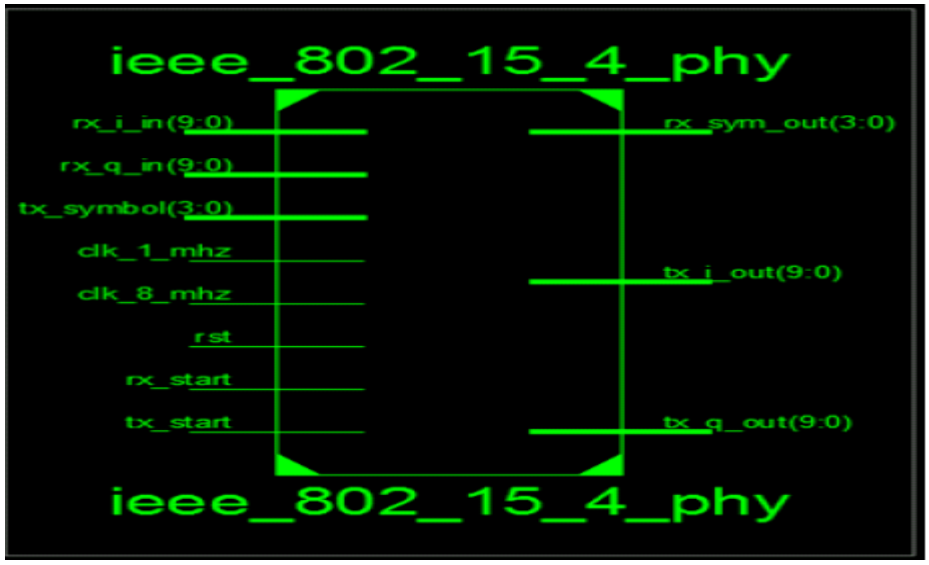

Figure 3: RTL schematic of Zigbee Transreceiver

The "clk_1_mhz" and "clk_8_mhz" are clock frequencies of 1 MHz and 8 MHz respectively. An input ports are consists of "rst", "tx_symbol(3:0)", "tx_start", "rx_start", "rx_i_in(9:0)", "rx_q_in(9:0)",. The "tx_i_out (9:0)" and "tx_q_out (9:0)" are output ports of I-phase signal and Q-phase signal respectively.

B. Design Utilization Summary :

Table 4: Design Utilization Summary of Zigbee Transreceiver

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	320	2443200	0%
Number of Slice LUTs	2526	1221600	0%
Number of fully used LUT-FF pairs	60	2786	2%
Number of bonded IOBs	18	850	2%
Number of BUFG/BUFGCTRLs	2	128	1%
Number of DSP48E1s	6	2160	0%

The Table 4. above shows the Design utilization summary for Zigbee Transreceiver. The design uses 320 slice registers out of 2443200 , 2526 slice LUT's out of 1221600 & 18 bounded IOB out of 850 available slices.

5. CONCLUSION:

A Zigbee Transceivers Transmitter and Receiver Block is enforced on Xilinx ISE 13.1 and verified success. The implementation of transmitter and Receiver is finished on Xilinx's Spartan 3 XC 3S200 FPGA. the data transmission and reception is additionally verified on FPGA by LED's & board switches. The modelsim simulator is employed to perform simulations. The waveforms matches with theoretical expectations.

6. REFERENCES:

1. IEEE Standard for Local and Metropolitan Area Networks-Part 15.4: Low-Rate Wireless Personal Area Networks (LRWPANs), IEEE Computer Society Std.
2. Newnes, Farahani. S, "Zigbee Wireless Networks and Transceivers," USA, 2008.
3. S. Bluetooth, "Bluetooth specification," 2007.
4. Z. Alliance, "ZigBee Alliance," WPAN industry group, The industry group responsible for the ZigBee standard and certification, 2010.
5. IEEE Standard for Local Area Networks-Part 11: Wireless Local Area Networks, IEEE Computer Society Std.
6. J.-S. Lee, Y.-W. Su, and C.-C. Shen, "A Comparative Study of Wireless Protocols: Bluetooth, UWB, ZigBee, and Wi-Fi," Taipei, Taiwan, 2007, pp. 46 – 51
7. Rafidah Ahmad, Othman Sidek, Wan Md. Hafizi Wan Hassin, Shukri Korakkottil Kunhi Mohd, and Abdullah Sanusi Husain, "Verilog-Based Design and Implementation of Digital Transmitter for Zigbee Applications," Int. J. Emerg. Sci., 1(4), 723-734, December 2011.
8. Rahmani. E, "Zigbee/IEEE 802.15.4", Univerity of Tehran, 2005.
9. Shuaib. K, Alnuaimi. M, Boulmalf. M, Jawhar. I, Sallabi. F and Lakas. A, "Performance evaluation of IEEE 802.15.4: Experimental and simulation results", Journal of Communications, 2, 4(2007): 29-37
10. Kisiel, Sahota, Swaminathan, "Quadrature Amplitude Modulation: simulation study",School Of Engineering Science Simon Fraser University, Canada , 2005.
11. John. G. Proakis, "Digital Communications", McGraw Hill Inc, New York , 1995.
12. Vaishali K. Patil, PROF. Parag Jawarkar," VERILOG BASED DESIGN AND SIMULATION OF PHYSICAL LAYER OF ZIGBEE TRANSRECEIVER", International Journal of Engineering Science & Advanced Technology, Volume-4, Issue-6, 013-016.
13. Vivek P. Supare, Bharati B. Sayankar and Pankaj Agrawal, " Design & Implementation of MQAM based IEEE 802.15.4/ZigBee Tranceiver using HDL", 2015 International Conference on Smart Technologies and Management for Computing, Communication, Controls, Energy and Materials (ICSTM), 6 - 8 May 2015. pp.523-526.