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Comparative study of Built in Self Test for memory

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ABSTRACT

The VLSI manufacturing technology advances has made possible to put millions of transistors on a single die. This advancement in IC technology enabled the integration of all the components of a system into a single chip. With the trend of SOC technology, high density and high capacity embedded memories are required for successful implementation of the system. Depending upon the application and design, much of the low yield can be attributed to faults in the memory. In this paper we study the BIST (Built in self test) for memory testing and compare the algorithms for testing.

Key Words: VLSI, IC, SOC, BIST

INTRODUCTION:

Due to the limitations of the fabrication process, many components of the chip are prone to structural errors which may lead to improper functioning of the chip. To detect these errors before the chip goes in to a system is very important to reduce the risk of the system failing field trials.

The different components that can be affected by these fabrication errors are standard cells (gates), wires and high density memories. Based on the nature of the build and functionality of these components, the testing process for these errors can be grouped as 1) logic testing (standard cells and wires) and 2) memory testing (memories).

The test process is generally done by the external device called ATE (Automatic Test Equipment). The ATE applies a pre-generated set of inputs called as test vectors to the chip and compares the outputs to a predefined set of expected values. The disadvantages of using ATE for testing are cannot perform At-Speed testing.
Very expensive i.e. cost increases in proportion to the number of test vectors.

One ATE machine can only test one chip at a time there by causing delays for systems that are to be manufactured on a large scale.

These disadvantages can be overcome by BIST. BIST requires a small amount of extra hardware to be inserted into the chip. The basic concept of BIST involves the design of test circuitry around a system that automatically tests the system by applying certain test stimulus and observing the corresponding system response. The definition of the BIST is given as the ability of logic to verify a failure-free status automatically, without the need for externally applied test stimuli and without the need for the logic to be part of a running system.

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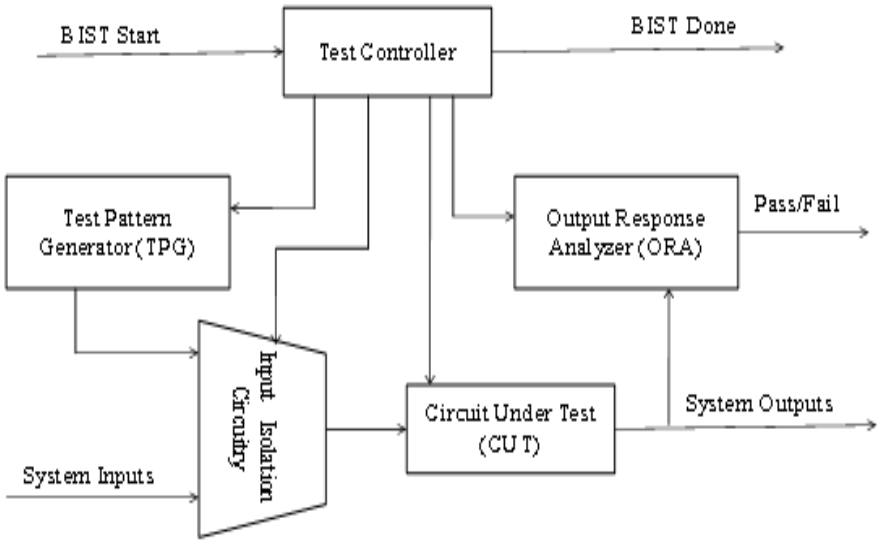

Figure 1: Basic BIST architecture

The various components of BIST hardware are the test pattern generator (TPG), the test controller, circuit under test (CUT), input isolation circuitry and the output response analyzer (ORA). This is shown in the figure above.

1.Test Pattern Generator (TPG):

Responsible for generating the test vectors according to the desired technique (i.e. depending upon the desired fault coverage and the specific faults to be tested for) for the CUT. Linear feedback shift register (LFSR) and pseudo random pattern generator (PRPG) are the most widely used TPGs.

2. Test Controller

It is responsible for controlling the other components to perform the self test. The test controller places the CUT in test mode and allows the TPG to drive the circuit's inputs directly. During the test sequence, the controller interacts with the ORA to ensure that the proper signals are being compared. The test controller asserts its single output signal to indicate that testing has completed, and that the ORA have determined whether the circuit is faulty or fault-free.

3. Output Response Analyzer (ORA)

Responsible for validating the output responses i.e. the response of the system to the applied test vectors needs to be analyzed, also, a decision is made about the system being faulty or fault-free. LFSR and multiple input signature register (MISR) are the most widely used ORAs.

Advantages of BIST:

Vertical testability: The same testing approach could be used to cover wafer and device level testing, manufacturing testing as well as system level testing in the field where the system operates.

Reduction in testing costs: The inclusion of BIST in a system design minimizes the amount of external hardware required for carrying out testing significantly.
In-field testing capability: Once the design is functional and operating in the field, it is possible to remotely test the design for functional integrity using BIST, without requiring direct test access.

Robust/repeatable test procedures: The use of ATE moves the CUTs onto a testing framework. Due to its mechanical nature, this process is prone to failure and cannot guarantee consistent contact between the CUT and the test probes from one loading to the next. In BIST, this problem is minimized due to the significantly reduced number of contacts necessary.

Delay testing: Can be used for delay testing as it can be used in real time.
Support concurrent testing
Testing during operation and maintenance
Dynamic properties of the circuit can be tested at speed

Disadvantages of BIST:

Area overhead: The inclusion of BIST in a particular system design results in greater consumption of die area when compared to the original system design. This may seriously impact the cost of the chip as the yield per wafer reduces with the inclusion of BIST.

Performance penalties: The inclusion of BIST circuitry adds to the combinational delay between registers in the design. Hence, with the inclusion of BIST the maximum clock frequency at which the original design could operate will reduce, resulting in reduced performance.

Additional design time and effort: During the design cycle of the product, resources in the form of additional time and man power will be devoted for the implementation of BIST in the designed system.

Added risk: What if the fault existed in the BIST circuitry while the CUT operated correctly. Under this scenario, the whole chip would be regarded as faulty, even though it could perform its function correctly.

The advantages of BIST outweigh its disadvantages. As a result, BIST is implemented in a majority of the electronic systems today, all the way from the chip level to the integrated system level.

BIST Types

They are two type of BIST:

1. LBIST (Logical Built in Self Test)
2. MBIST (Memory Built in Self Test)

1. Logical BIST (LBIST)

Today's SOCs can contain hundreds of memories, several types of logic, dozens of functional blocks obtained from diverse sources, and multiple clocks operating at multiple frequencies. This brings in its wake problems of defining a proper test strategy, optimizing test costs and the time required for testing. External access, embedded self-tests and diagnostics go a long way towards helping solve the test challenge.

Logic BIST makes itself a valuable, if not an indispensable tool. One of LBIST's greatest virtues is its ability to test a circuit at its full operating speed. Something that even some very expensive external ATE systems cannot do. Further, "at-speed" testing, as it is called, has become essential for submicron chips. LBIST is based on the scan method as the fundamental design for testability (DFT) technology. LBIST, which is designed for testing random logic, typically employs a PRPG to generate input patterns that are applied to the device's internal scan chain, and a MISR for obtaining the response of the device to these test input patterns as shown in the figure 2.3. An incorrect MISR output indicates a defect in the device.

2. **Memory BIST (MBIST)**

With the advent of deep-submicron VLSI technology, core-based SOC design is attracting an increasing attention. On an SOC, popular reusable cores include memories, processors, input/output circuits, etc.

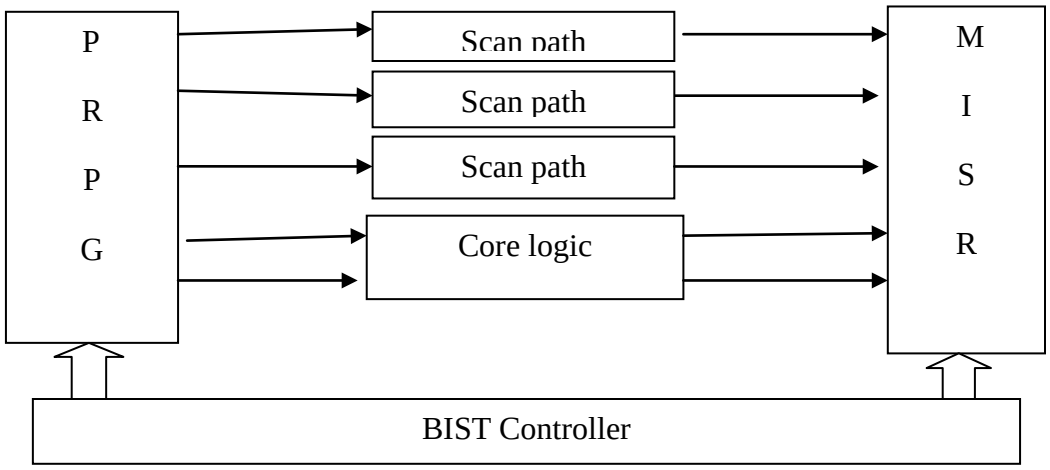

Figure 2: Basic methodology for Logic BIST

Digital systems are composed of data paths, control paths and memories. Defects in memory arrays are generally due to shorts and opens in memory cells, address decoder and read/write logic. These defects can be modeled as single and multi cell memory faults. The dominant use of embedded memory cores along with emerging new architectures and technologies make providing a low cost test solution for these on chip memories a very challenging task. The addition of extra circuitry to facilitate testing of memory chips, called DFT, or to allow the test mechanism to be completely contained within the chip, called BIST, has become of interest. MBIST, as its name implies, is used specifically for testing memories. It typically consists of test circuits that apply, read, and compare test patterns designed to expose defects in the memory device.

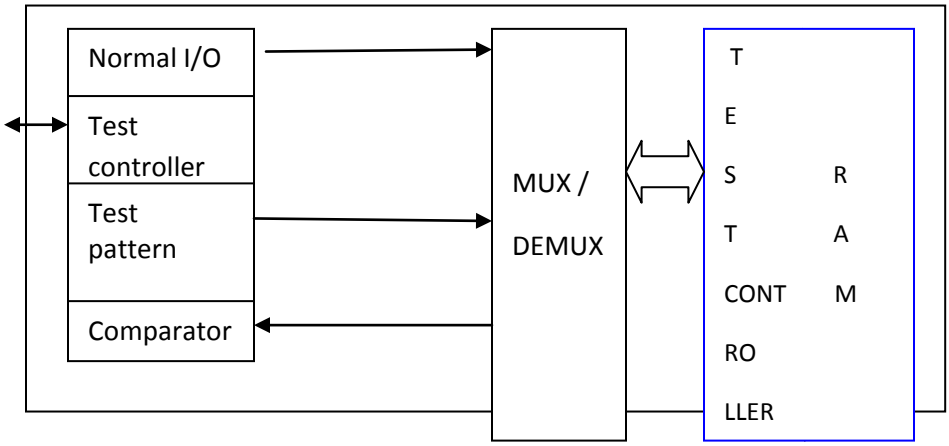

Figure 3: Memory BIST Architecture

MBIST has been proven to be one of the most cost-effective and widely used solutions for memory testing for the following reasons: no external test equipment, reduced development efforts, tests can run at circuit speed to yield a more realistic test time, on-chip test pattern generation to provide higher controllability and observability.

There now exists a variety of industry-standard MBIST algorithms, such as the walking 1/0 algorithm, march algorithm, the checkerboard algorithm, and the varied pattern background algorithm. With MBIST, the entire memory testing algorithm is implemented on-chip, and operates at the speed of the circuit, which are 2 to 3 orders of magnitude faster than a conventional memory test. Most MBIST schemes exploit the parallelism within the memory device to achieve a massive reduction in test time. This is done by a test mode where more than one memory cell is accessed with each address, usually by accessing the entire row of cells on a word line for a single read or write operation. For n cells in the memory, with √n rows √n columns, this reduces test time by a √n factor.

The memory BIST is similar to the basic BIST circuit, where CUT is replaced with the RAM. Additional block called controller is needed. A Controller is a hardware realization of a selected memory test algorithm, usually in the form of a Finite State Machine (FSM). The MBIST figure is shown in the above figure.

BIST techniques

BIST for logic testing and memory testing are of completely different structure because of the nature of structural faults present in them.

The types of errors targeted in Logic BIST (LBIST) are

Stuck – at – faults (SAF)
Transition faults (targeted by at speed testing)

The types of errors targeted in memories (MBIST) are

Stuck – At – Faults (SAF)
Transition Faults (TF)
Address Decoder Faults (ADF)
Coupling Faults (CF)
Data Retention Faults (DTF)

Memory chip test algorithms:

A test algorithm is a finite sequence of test elements. A test element contains a number of memory operations (access commands), data pattern (background) specified for the read operation, address (sequence) specified for the read and write operations. Table 1 gives summary of various test algorithms that have been actually implemented in modern memory BIST circuitries. We divided these test algorithms into two groups: Classical tests and March-based tests.

1. Classical test algorithms:

Classical test algorithms are either (1) simple, fast but have poor fault coverage, such as Zero-one, Checkerboard; or (2) have good fault coverage but complex and slow, such as Walking, GALPAT, Sliding Diagonal, Butterfly, MOVI, and etc.. Due to these imbalanced conflicting traits, the popularity of these algorithms is decreases.

2. March-based test algorithms:

A March-based test algorithm is a finite sequence of March elements. A March element is specified by an address order and a number of reads and writes. Examples of some March based tests are MATS, MATS+, Marching 1/0, March C-, March Y, March A, March B, and etc. Since March-based tests are all simple and possess good fault coverage, they are the dominant test algorithms implemented in most modern memory BIST

Table 1: Summary of memory test algorithms

Algorithm	Fault Coverage					Test Time	
	AF	SAF	TF	CF	Others	Order	1M mem.
Zero – One	-	L	-	-		O (n)	0.42s
Checkerboard	-	L	-	-	Refresh	O (n)	0.52s
Walking 1/0	L	L	L	L	Sense amplif. rec.	O (n^2)	2.5d
GALPAT	L	L	L	L	Write recovery	O (n^2)	5.1d
GALROW	LS	L	L	L	Write recovery	O (n. v n)	7.2m
GALCOL	LS	L	L	L	Write recovery	O (n. v n)	7.2m
Sliding Diag.	LS	L	L			O (n. v n)	10s
Butterfly						O (n. log 2n)	3.6m
MATS	DS	D	-	-		O	0.42s
MATS+	D	D				(n)	0.52s
Marching 1/0	D	D	D	-		O (n)	1.5s
MATS ++	D	D	D	-		O (n)	0.63s
MARCH X	D	D	D	D	Unlinked CFins	O (n)	0.63s
MARCH C-	D	D	D	D	Unlinked CFins	O (n)	1.0s
MARCH A	D	D	D	D	Unlinked CFins	O (n)	1.6s
MARCH Y	D	D	D	D	Linked TFs	O (n)	0.85s
MARCH B	D	D	D	D	Linked TFs	O (n)	1.8s
						O (n)	
MOVI	D	D	D	D	Read access time	O (n. log 2n)	3.3h
3-coupling	D	D	D	D	3-coupling faults	O (n. log 2n)	54s
Paragon	D	D	D	D	Operational faults	O (n^2)	20d

L = Locate LS = Locate Some D= Detect DS = Detect Some 'n' indicates the number of inputs.

Simulation Result Using ModelSim Tool:

1. Memory

At first we had simulated a normal memory without any fault the simulation waveform is shown in below figure

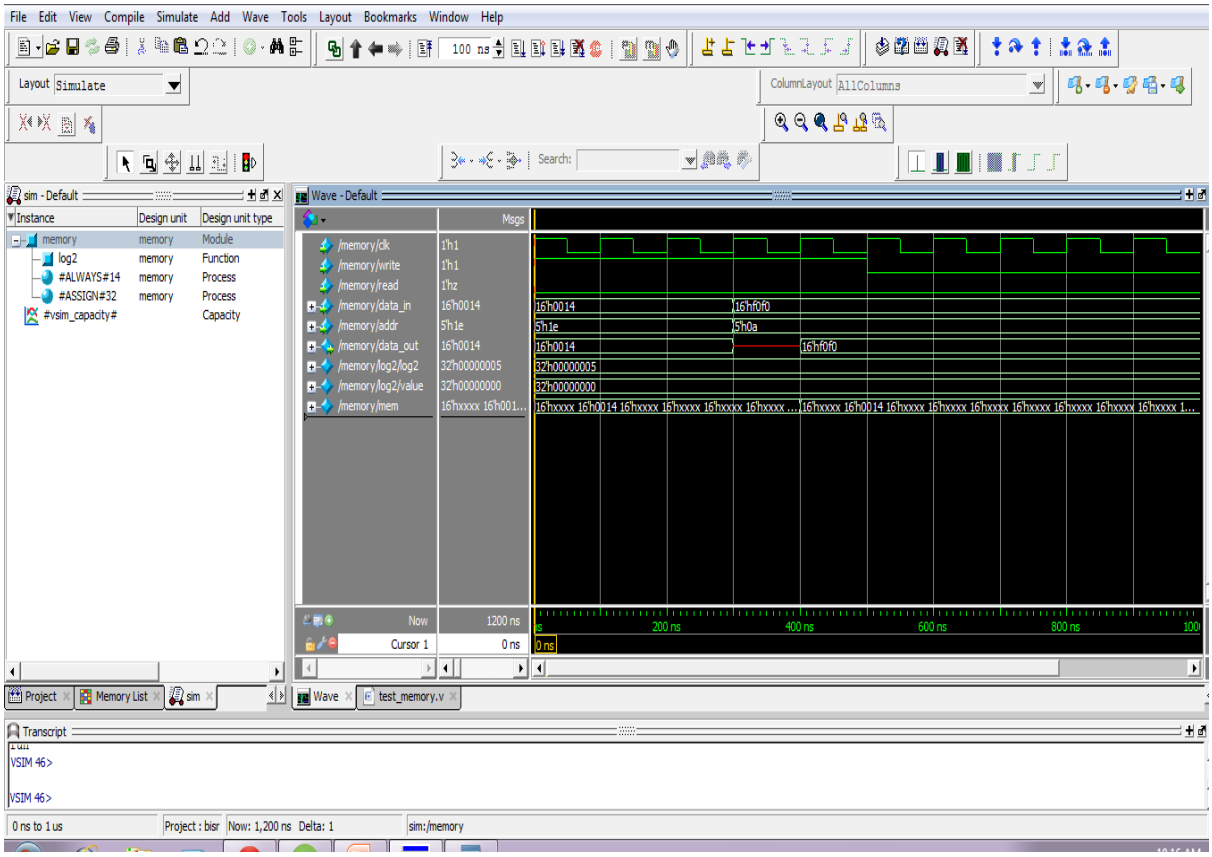

Figure 4: Simulation waveform of a memory

2. Top BIST module

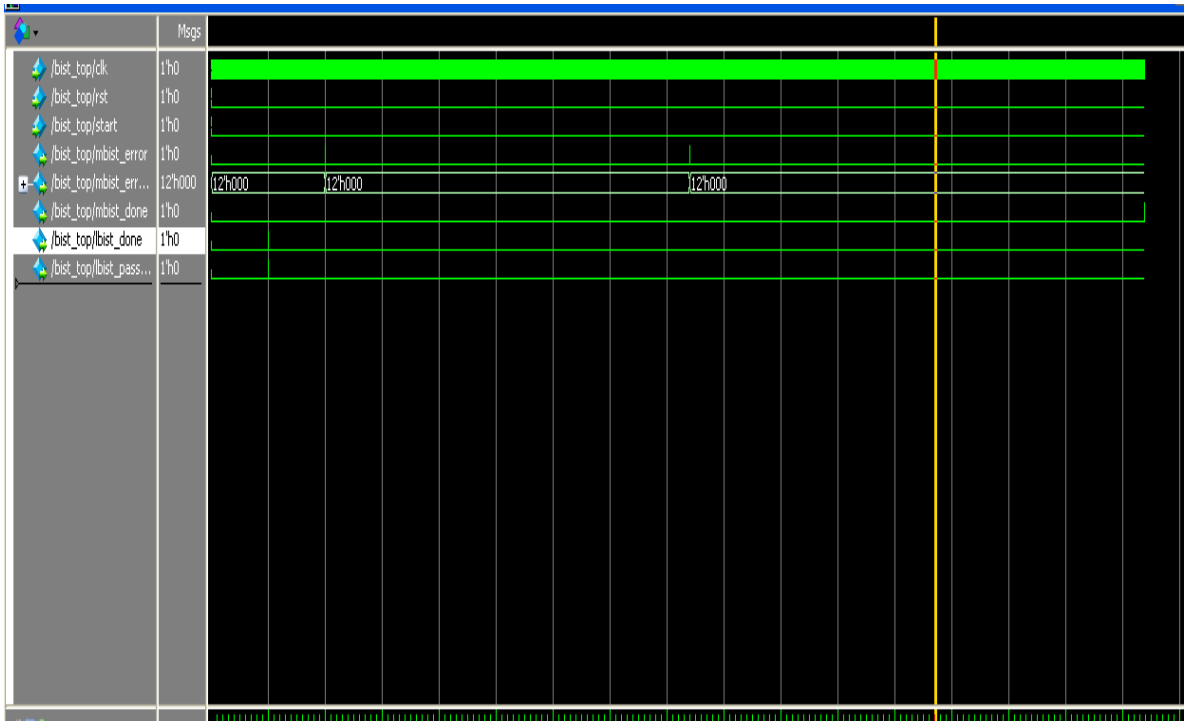

Figure 5: Simulation waveform for top BIST compressed results

3. Simulation waveform of MBIST

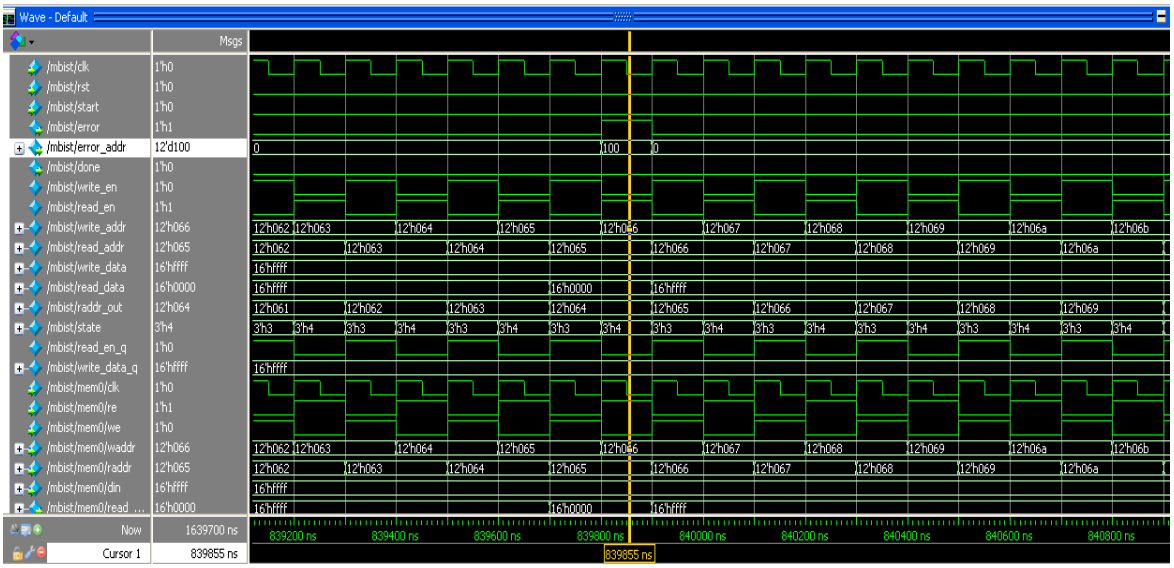

Figure 5: Simulation for Stuck at 0 at 100

The above figure shows the MBIST error i.e, Stuck at 0 at the memory address 100

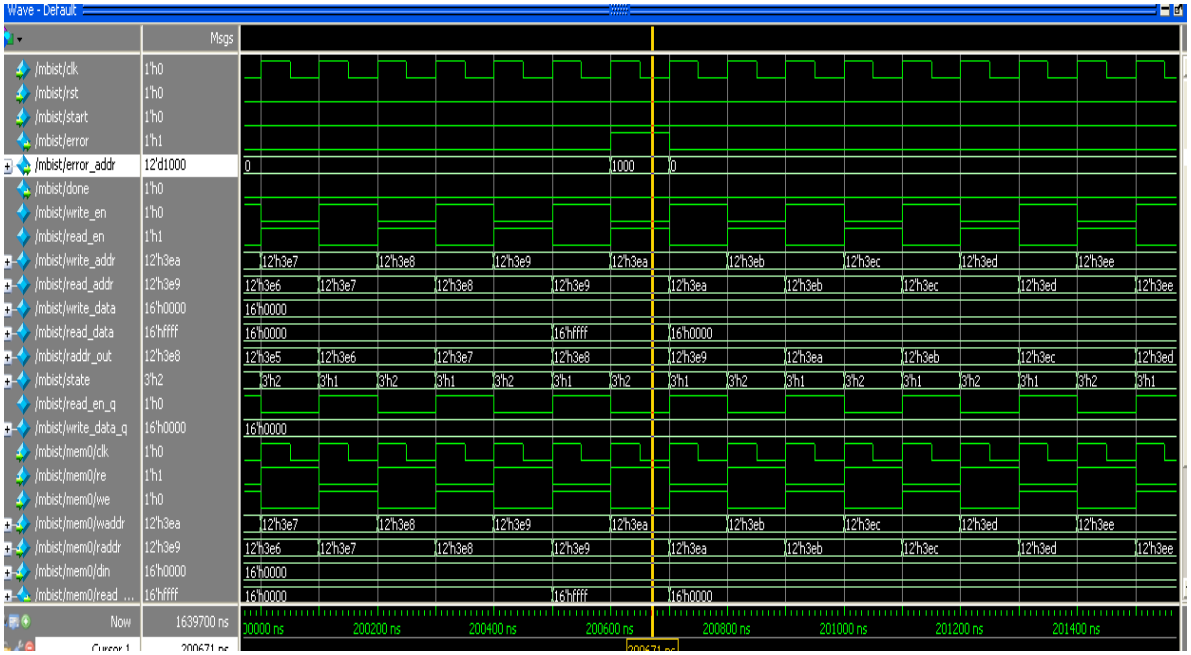

Figure 6: Simulation waveform for Stuck at 1 at 1000

The above figure shows the MBIST error i.e, Stuck at 0 at the memory address 1000

CONCLUSION

An efficient programmable BIST strategy and selectable redundancy has been presented in this paper. It is designed flexible that users can select operation modes of SRAM.

As these benefits are obtained at low area cost, the proposed memory BIST becomes highly attractive not only for test chips dedicated to new memory and/or process debug but also for integrating it into final products. The function of BIST has been verified by the

post simulation. The BIST can work at up to 150MHz at the expense of 20% greater area.

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