ISSN: 2348 - 2117

International Journal of Engineering Technology and Computer Research (IJETCR)
Available Online at www.ijetcr.org
Volume 3; Issue 2; Page No. 181-184

Semiconductor Memories and its Faults

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ABSTRACT
In this paper, different semiconductor memories are presented. Semiconductor memory is an electronic data storage device, often used as computer memory, implemented on a semiconductor-based integrated circuit, system on chip (SoC) or embedded memories. It is made in many different types and technologies. The idea of this paper is to give brief description of SRAM and DRAM. This paper also gives an idea about different faults in memory.

Key words: Semiconductor memories, SRAM, DRAM, Memory faults

INTRODUCTION

Memory is a means for storing data or information in the digital form. It is made up of storage locations in which numeric or alpha numeric information or programs may be stored [1].

Semiconductor memory is an electronic data storage device, often used as computer memory, implemented on a semiconductor-based integrated circuit, system on chip (SoC) or embedded memories. Semiconductor memory has the property of random access, which means that it takes the same amount of time to access any memory location, so data can be efficiently accessed in any random order.[2]

There are two basic kinds of semiconductor memory. First one is Static RAM (SRAM) consists of flip-flops, a bistable circuit composed of four to six transistors. Once a flip-flop stores a bit, it keeps that value until the opposite value is stored in it. SRAM gives fast access to data, but it is physically relatively large. It is used primarily for small amounts of memory called registers in a computer's central processing unit (CPU) and for fast "cache" memory.

Other is Dynamic RAM (DRAM) stores each bit in an electrical capacitor rather than in a flip-flop, using a transistor as a switch to charge or discharge the capacitor. Because it has fewer electrical components, a DRAM storage cell is smaller than SRAM. However, access to its value is slower and, because capacitors gradually leak charges, stored values must be recharged approximately 50 times per second. Nonetheless, DRAM is generally used for main memory because the same size chip can hold several times as much DRAM as SRAM [2].

1. Static Ram:

Static random access memory (SRAM) is a semiconductor memory which uses bistable latching circuitry to store single bit of data. SRAM exhibits data remanence [4], but it is still volatile in the conventional sense that data is eventually lost when memory is not powered.

The schematic and layout of a six-transistor SRAM memory cell is seen in Fig. 1.This is, as its name implies, static, meaning that as long as power is applied to the cell it will remember its contents (unlike the DRAM cell, which loses its memory after a short time). The basic cross-coupled inverter latch should be recognized in the topology. To access the cell, the word line goes high and turns on the access MOSFETs. The bit lines are driven in complementary directions with a "strong" driver for writing. When the word line goes low, the datum is latched in the cell [5].

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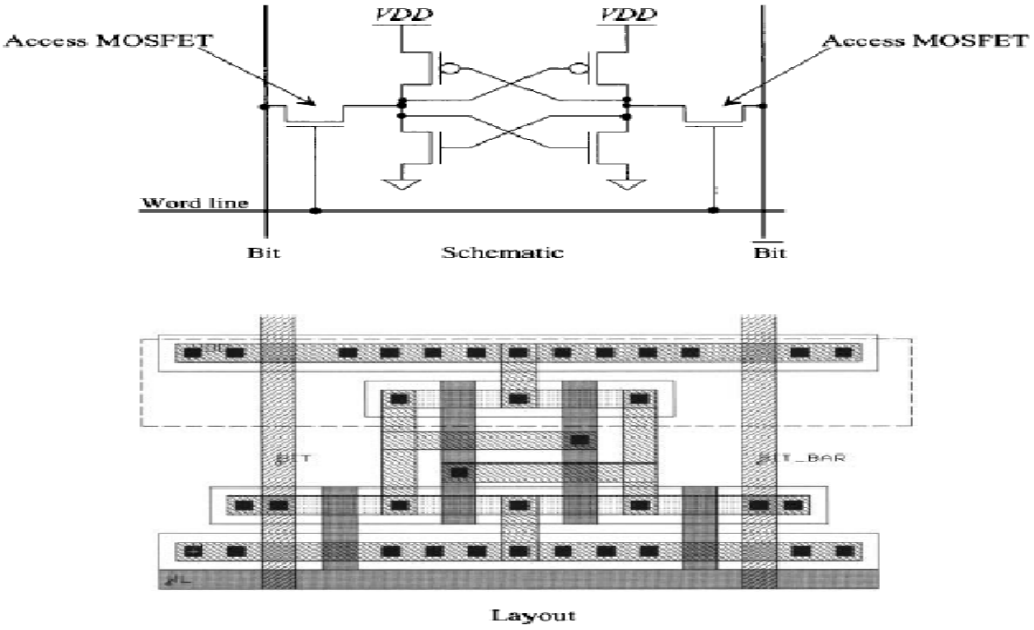

Figure 1: The six transistor SRAM memory cell

A disadvantage of a computer with static RAM is that the RAM takes up a lot of physical space. A static RAM chip needs four to six transistors to store a bit of information. Other disadvantage is SRAM is much more costly than a DRAM

2. DYNAMIC Ram:

Dynamic random-access memory (DRAM) is a type of random-access memory that stores information in capacitor within an integrated circuit. It stores one bit of data in a single capacitor. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, 0 and 1. Since even "non-conducting" transistors always leak a small amount, the capacitors will slowly discharge, and the information eventually fades unless the capacitor charge is refreshed periodically [5].

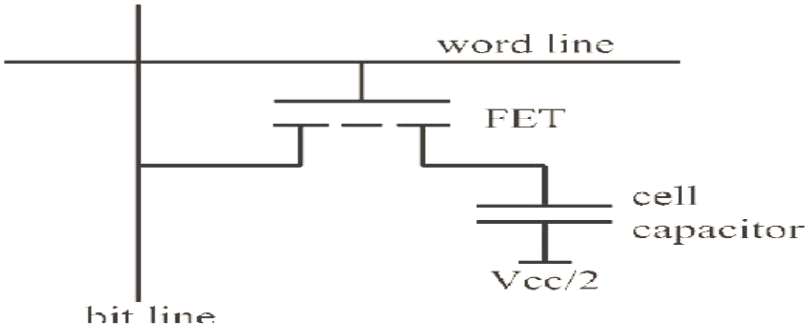

Figure 2a: DRAM memory cell

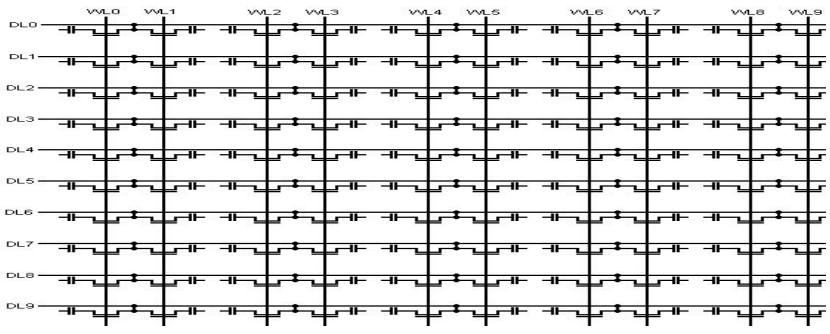

Figure 2b: DRAM memory

The advantage of DRAM is in its structural simplicity: only one transistor and a capacitor are required per bit, compared to four or six transistors in SRAM. This allows DRAM to reach very high densities. The transistors and capacitors used are extremely small; billions can fit on a single memory chip.

The main disadvantage of DRAM is in its data storage ability. Unlike flash memory, DRAM is volatile memory (vs. non-volatile memory), since it loses its data quickly when power is removed.

The schematic of a single cell of DRAM is shown in Fig.2a, which is a combination of capacitor and a transistor. The array of such cells creates a DRAM memory chip which is shown in fig.2b.

3. FAULTS

A fault is physical defect which may or may not cause failure; where failure in a system is deviation from specified behavior [6].

In memories many faults are there which are sometime due to functional failure of system sometime they are because of detects that occur at the time of fabrication. Memories fault are broadly classified as

1) Logical Faults
2) Physical faults

There is large number of logical faults in memory. However, the following faults called "reduced functional faults" are sufficient for functional memory testing study.

1) Stuck at fault
2) Transition fault
3) Coupling fault
4) Bridging fault
5) Neighbour pattern sensitive fault
6) Address decoding fault

Stuck-at-fault in memory is the one in which the logic value of a cell (or line in the sense amplifier or driver) is always 0 or always 1.

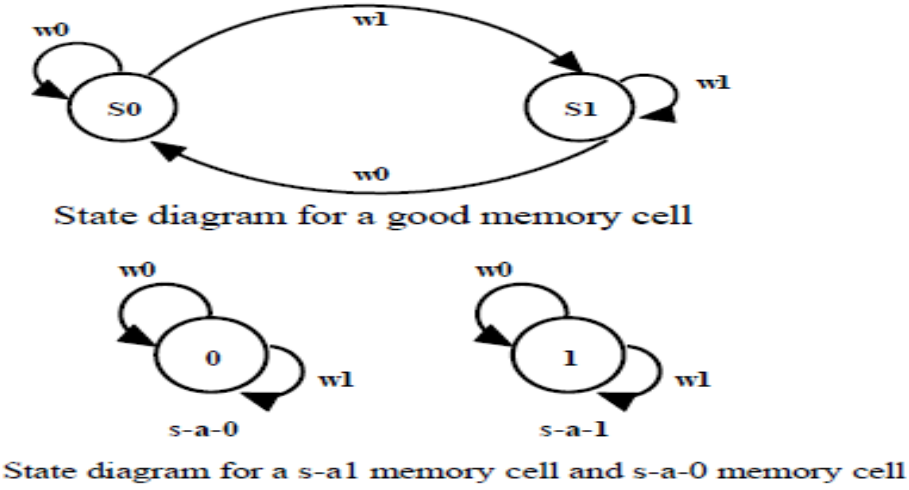

Figure 3: State diagram of memory chip without and with stuck at faults

In transition fault a cell fails to make a (0 to 1) transition or a (1 to 0) transition when it is written; up transition fault is denoted as (↑|0) and a down transition fault is denoted as (↓|1)

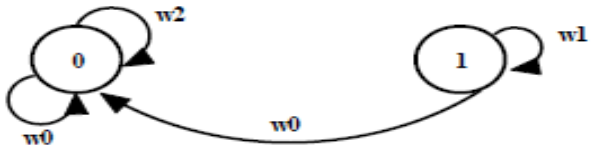

Figure 4: State diagram of memory chip with transition at faults

Coupling fault, as the name suggests, implies deviation from normal behavior of a cell because of coupling with others. As there can be exponential number of combinations of coupling of a cell with others cells, we assume that in coupling faults a faulty cell can get coupled with another faulty cell. In other words, in the widely used coupling fault model it is assumed that any "two" cells can couple and normal behavior changes in these two cells; it is called 2-coupling fault model. So if

there are n cells in a memory then there can be nC2 number of 2-coupling faults.

A bridging fault is a short circuit between two or more cells. As in the case of coupling faults, to keep the number of faults within a practical number, it is assumed that only two cells can be involved in a bridging fault. There are two types of bridging faults.

1) AND bridging fault ANDibi,j (involving cells i and j) which results in values in cells i and j to be logic AND of the values in these cells under normal condition. AND bridging fault is represented by (vi, vj | viANDvj, viANDvj) where the first two places represent the values in cells i and j under normal condition and the two values following "|"represent the values in cells i and j under AND bridging fault. (0,0|0,0),(0,1|0,0),(1,0|0,0),(1,1|1,1) , are the four types of AND bridging faults possible.

2) OR bridging fault ORbfi,,j (involving cells i and j) which results in values in cells i and j to be logic OR of the values in these cells under normal condition. (0,0|0,0),(0,1|1,1),(1,0|1,1),(1,1|1,1) are the four types of OR bridging faults possible.

One of the most important and different kind of fault in memory compared logic gate circuits is neighborhood pattern sensitive faults (NPSFs). As memory cells are very close to each other, the cells behave normally except for certain patterns in the neighborhood cells. For example, if a cell i has 0 and all the neighboring cells have 1, then the value of cell i may be pulled up to 1. It is obvious that given a cell there can be infinite number of neighborhood combinations.

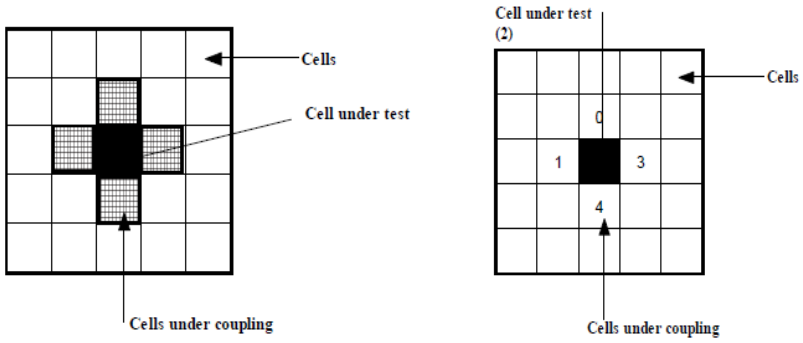

Figure 4: memory chip with neighbor pattern sensitive fault

Address decoding fault is one in which with some address the data integrity is not maintained. From the context of memory testing four types of faults are considered in address decoder (for both reading and writing)

- No cell is accessed for a certain address
- No address can access a certain cell
- With a particular address, multiple cells are simultaneously accessed.
- A particular cell can be accessed with multiple addresses.

4. Conclusion

In this paper we have presented that memory can store the data in the form of voltages or currents. With the concern to the space it is more suitable to use DRAM cells. We had also discussed different faults in the semiconductor memories. These faults are basically generated in the fabrication or while functioning of the cell, to overcome the faults in semiconductor memories different test are done while functioning and at the manufacturing level also.

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